

Analog Television, WiMAX and DVB-H on the Same SoC Platform

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Abstract—This paper presents a SW reconfigurable platform, capable of executing in real time both analog and digital television protocols as NTSC, PAL, SECAM and DVB-H. Our platform is also capable of executing WiMAX at 2.9 Mbps in real time, as well as other mobile telephony protocols like 3G UMTS or CDMA200. SW reconfigurability and low power consumption makes our platform suitable for mobile applications. Current analog and digital television systems have been developed in a combination of analog and/or digital hardware due to high computational processing requirements. They are also mostly limited to a single function either analog TV or, digital TV. DSPs in these systems have been limited to speech coding and orchestrating the custom hardware blocks. Despite the fact that in high-performance systems there may be over 2 million logic gates required to implement physical layer processing, the implementation may take many months to finalize. After the logic design is complete, any errors in the design may cause up to a 9 month delay in correcting and refabricating the device. This labor intensive process is counter productive to fast development cycles. In our approach, the entire physical layer is executed in SW using the SB3011 DSP from Sandbridge Technologies [1] allowing fast development cycles and support of multiple functions. (*Abstract*)

I. INTRODUCTION

As the microprocessors become more and more powerful, and the general purpose DSPs are replaced by more capable Systems on Chip able to execute billions of instructions per second, there is a normal trend to replace the hardware based implementation of communication systems with more flexible and easy to maintain SW applications. In the past few years, the mobile industry went through dramatic changes. The lifespan of a mobile phone becomes less than two years. In addition, there are two competing factors: first, the need of adding more communication and multimedia components on the same hand held device and second, the form factors is shrinking continuously. To

overcome these competing factors, some reconfigurability is needed. The Sandbridge software solution for implementing the physical layer for various communication systems while conserving the power consumption, proves to be an attractive solution.

Even if the digital TV is becoming increasingly attractive to provide mobile platforms with the capabilities of viewing TV broadcasting, the analog TV (NTSC, PAL, SECAM) is still the most common TV system. Therefore it is attractive, in our opinion, for the handheld device to be enabled with analog TV capabilities.

In the following, we present the system and real time implementation and performance of the analog TV, DVB-H and WiMAX on the same Sandbridge SW platform. All communication systems presented in this paper share the same high level system block diagram illustrated in Figure 1. the radio frequency signal is down converted and, the resulting base band (or low intermediate frequency) signal is digitized. From that point the entire signal processing is done digitally.

The paper is structured as follows: Section II describes the system implementation of the Analog Television, DVB-H and WiMAX. Section III includes the real time performance and conclusions. The references are listed in the last section.

II. SYSTEM DESCRIPTION

A. Analog TV

The system block diagram of the analog TV receiver [2] implemented in the SB3011 DSP is illustrated Figure 1. More system and algorithmic details are described in [3]. The received analog TV signal is first down converted to base band. The base band signal, or the composite video signal, is then digitized and passed to the DSP. From this stage, the entire video processing is executed digitally. In NTSC systems[2][5], each video frame consists of 2 color

fields or 525 lines. As shown in Figure 2. , the first 20 lines of color field I, is the field-blanking period that carries the vertical synchronization pulses. The vertical synchronization pulses indicate the start of a new video frame.

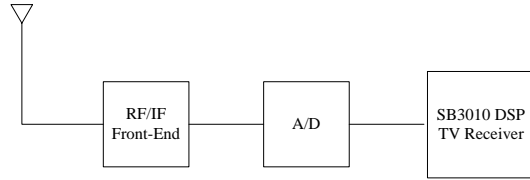


Figure 1. System Block Diagram of Analog TV Receiver.

The color field II starts from the middle of line 263, carrying another 20 lines for the second field-blanking period indicating the middle of the video frame. The rest of lines in color field I and II are the displayable video lines.

Figure 3. illustrates the detailed video line signal timing and DC level information [5]. The various information carried by the video line must be constructed at predefined signal levels and timing to allow the receiver to reconstruct the RGB signals correctly. Each displayable video line consists of the following two parts: The "Blanking Period" carrying the "Front Porch", the "Sync Tip" or horizontal sync pulse" and the "Back Porch" with 9 ± 1 cycles of color burst riding on it.

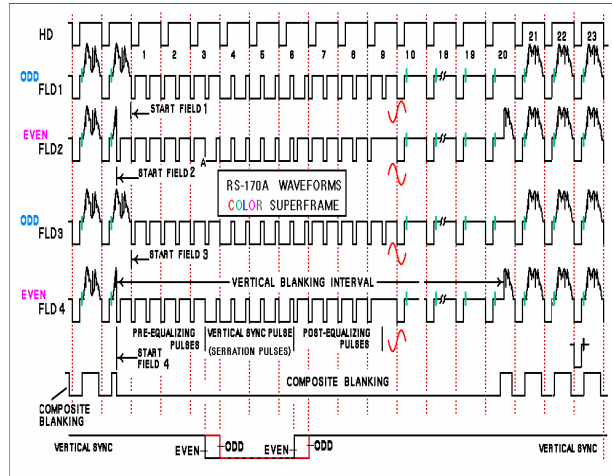


Figure 2. Color Field Blanking Sequence for NTSC

The horizontal sync pulse are used by the receiver for line synchronization and frequency / timing offset tracking purposes. The color burst is a sine wave reference signal at the chroma carrier frequency. It is used to extract the phase and frequency information for decoding the I/Q modulated chroma signal. Following the back porch, is the second part of the video line carrying the actual displayable video information (luminance and I/Q modulated chroma signal).

The analog TV receiver digital signal processing blocks implemented in the SB3011 DSP are illustrated in Figure 4. .

First, the horizontal synchronization and vertical synchronization sequences are detected and tracked by a Delay Lock Loop (DLL). The input video composite signal is then adjusted to achieve proper DC and IRE (Institute of Radio Engineers) scaling levels.

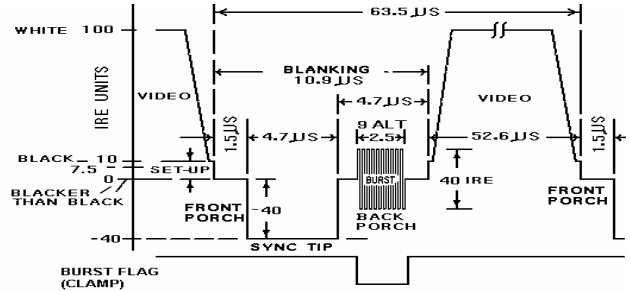


Figure 3. Details of Video Line Timing / Levels Information

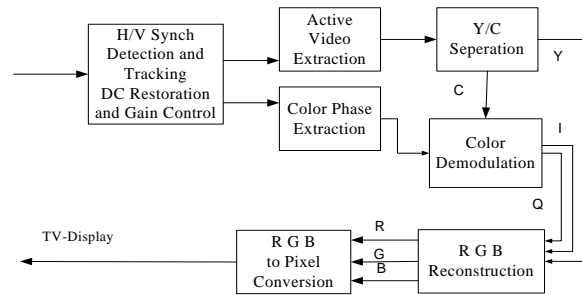


Figure 4. Signal Processing Block Diagram of NTSC Receiver

The active video information is extracted line-by-line as follows: the Y/C, or luminance and color, are separated first, followed by the color I/Q demodulation and the RGB signals reconstruction. The RGB signals for the current video frame are finally converted to pixels and displayed on the LCD screen.

B. Digital Video Broadcastin

Due to its robustness to multi-path propagation conditions and support for high data rates, Coded Orthogonal Frequency Division Multiplexing (COFDM) has become one of the most popular modulation techniques for indoor and outdoor broadband wireless data transmission [4]. Digital Video Broadcasting, Terrestrial and Handheld DVB-T/H are COFDM communication systems [6]

The block diagram of a generic DVB-H receiver is shown in Figure 5. The receiver includes all the blocks specific to OFDM receivers: coarse fractional frequency offset and integer frequency estimation, frequency tracking, coarse timing offset estimation and tracking, channel estimation, and correction, QAM symbol de-mapping. The block diagram of the base band processing for the 2k DVB-T receiver is illustrated in Figure 6. The detailed

implementation and real time performance for DVB-T/H is described in [9].

C. WiMAX

The WiMAX 2.9 Mbps is also an OFDM communication system. The OFDM signaling format was selected, in preference to other competing formats such as single-carrier (SC) CDMA, due to its superior multipath performance. It permits significant equalizer design simplification in order to support operation in non line of sight (NLOS) fading environments.

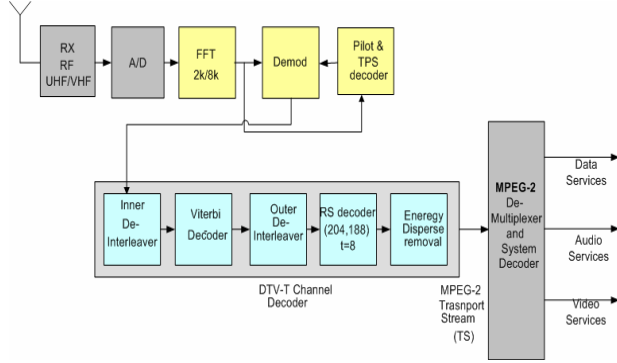


Figure 5. Generic DVB-T receiver block diagram.

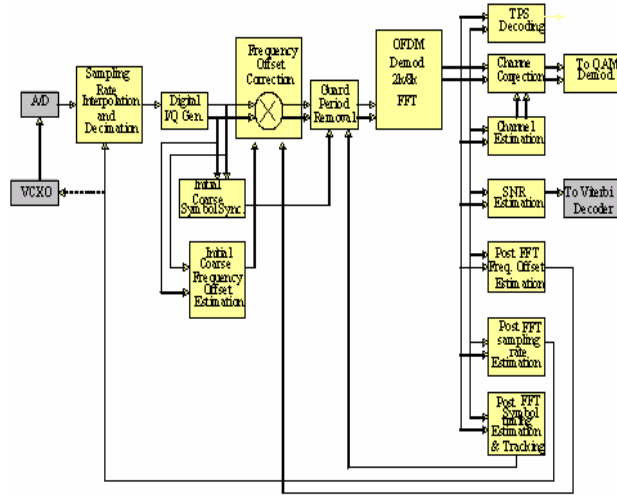


Figure 6. 2k DVB-T block diagram.

The WiMAX transmitter block diagram, as specified in IEEE 802.16 [7], is depicted in Figure 7. while the receiver block diagram is illustrated in Figure 9. All signal processing functions described in the block diagrams, after the analog to digital (AD) and before the digital to analog (DA) converters, are executed in SW including all the RF controls.

The OFDM demodulator which is the receiver front-end processing is shown in Figure 8. . The back-end signal processing block is the reverse of the transmitter pipeline. Note, for the 2.9 Mbps option, the RS decoder is not required.

The front-end signal processing block diagram follows: the inputs to the A/D converter are the I and Q base-band signals coming from the RF chip. The I/Q signals are first 2:1 decimated and filtered to the FFT sampling frequency F_s .

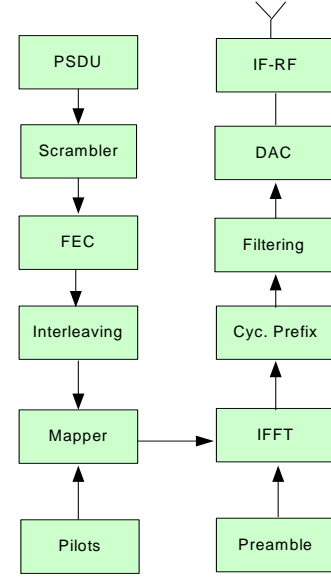


Figure 7. WiMAX Transmitter Block Diagram

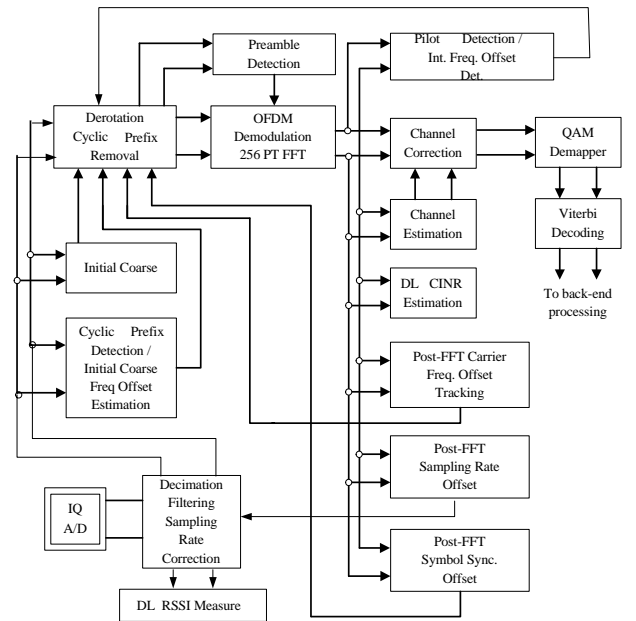


Figure 8. WiMAX processing blocks

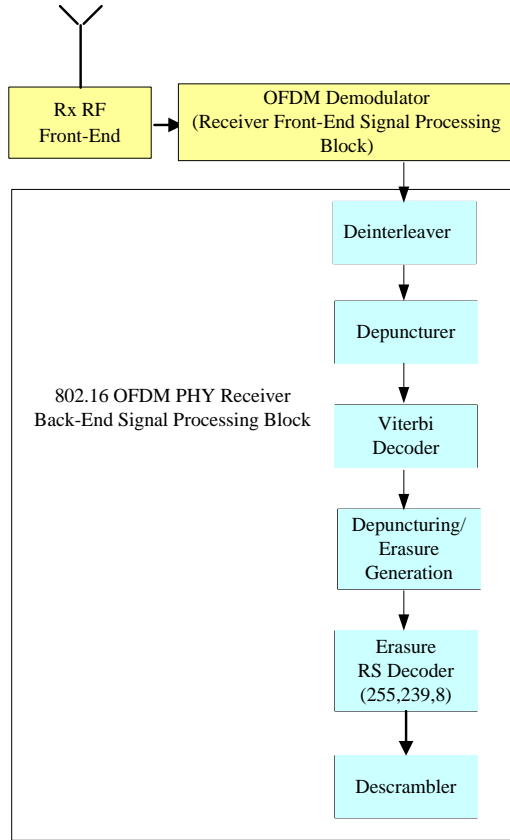


Figure 9. WiMAX Receiver Block Diagram

The FFT sampling frequency is proportional to the channel bandwidth BW as follows:

$$F_s = \text{floor}(n \times BW / 8000) \times 8000$$

In our implementation, $BW=7\text{MHz}$, $n=8/7$, $F_s=8\text{MHz}$, the ADC sampling frequency will be at $2 \times F_s=16\text{MHz}$.

The system, algorithms and software implementation details are described in [8].

III. PERFORMANCE AND CONCLUSIONS

The real time performance is illustrated in Figure 10.

The Analog TV, for 525 lines and 30 frames per second requires less than one SB3011 core.

WiMAX, at 2.9 Mbps for full frequency duplex (FDD) mode requires pretty much the entire processor, four cores.

DVB-H is defined in the standard for three modes of operation: 2, 4 and 8k. For the three modes of operation, at 250Kbps and 1.5Mbps bit rates, the total processing requirement is between a fraction of a processor up to less than one half of a processor.

We have shown that multiple communication protocols can coexist efficiently on the same software based development platform using the SB3011 processor. The entire development has been done using ANSI C, making the development process fast and easy to maintain.

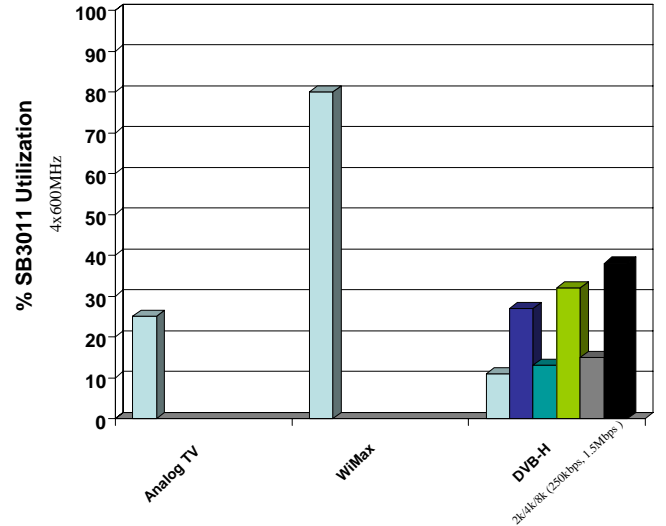


Figure 10. Performance results for SB3011 real time implementation.

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