Sandbridge's Software Defined Radio (SDR) Solution

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Agenda

Motivation for SDR

Multithreaded SDR Processor

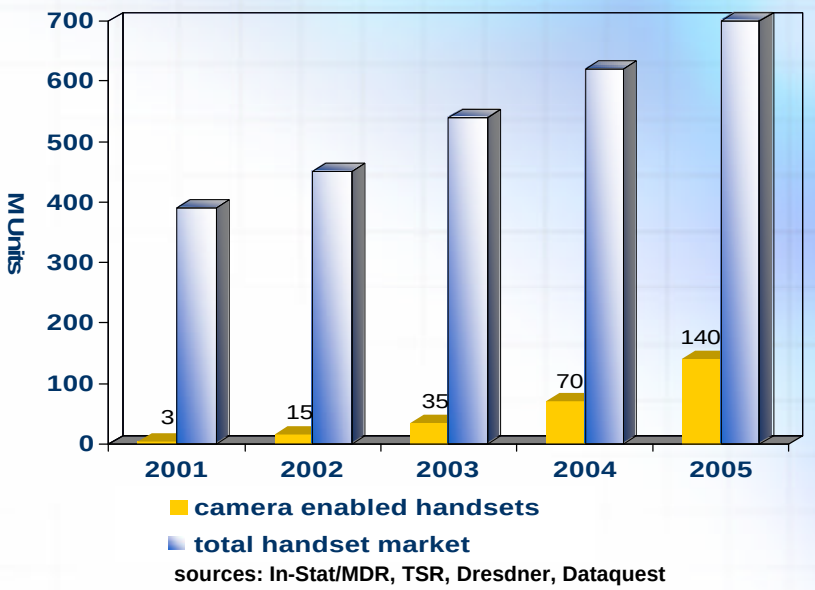
Software Development Tools

- Compiler
- Simulator
- IDE

Communications System Implementation

- 2Mbps WCDMA

What is it that we eventually carry with us ?



It has a color screen, camera, audio and antenna …

… but all features need high computing performance and ultra low power consumption

- Wireless communication 2G – 2.5G – 3G – WLAN – BT – etc.
  - GSM/IS-95a,b/IS-136/PDC/ iDEN – CDMA2k/GPRS/EDGE – FDD/TDD/TD-SCDMA/Jap.WCDMA/CDMA2k-3x– 802.11a,b,g
- Radio broadcast GPS – radio – TV – etc.
  - Location based services/911/tracking services – AM/FM/DAB – Sat./Terr.TV
- Encryption – decryption – media encode – media decode
- Games – speech to text – natural language processing

The Challenges of an Industry

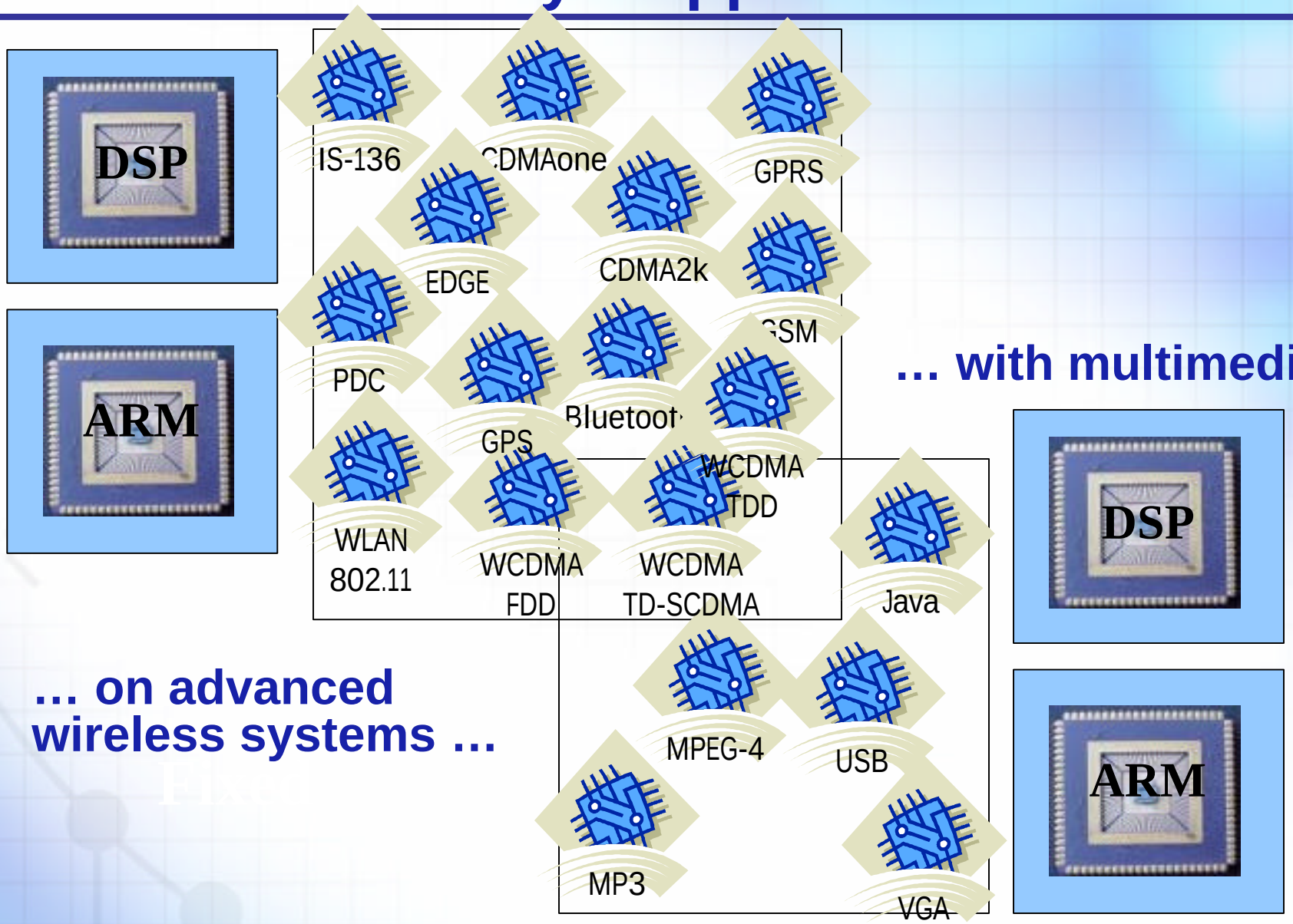
Cost

- 3G is >10x more complex than 2G
  - but cost should be same, or even less
- Convergence phone 2x complexity
  - WLAN, 2G, and 2.5G integration
  - Traditionally implemented in HW
- Moore's law reduces cost 50% every 18 months
  - 6 years until the wireless multimedia is a real consumer market

Time-to-market

- GPRS terminals were late
  - OEMs had to wait until bug free SoCs were available
- 3G terminals will be late
  - OEMs have to wait until bug free SoCs with 'reasonable' power consumption are available

A Whole Industry's approach failed …



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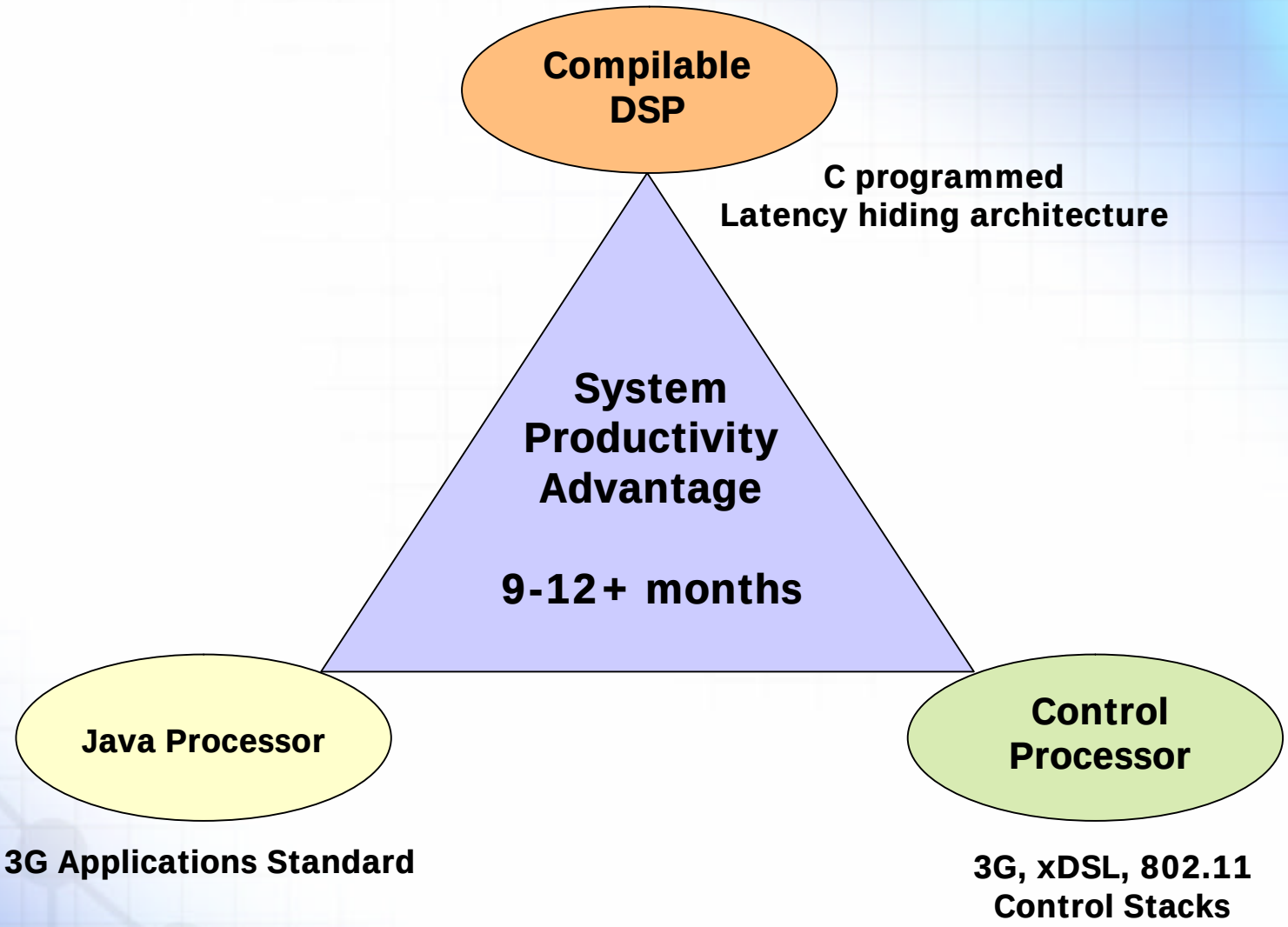
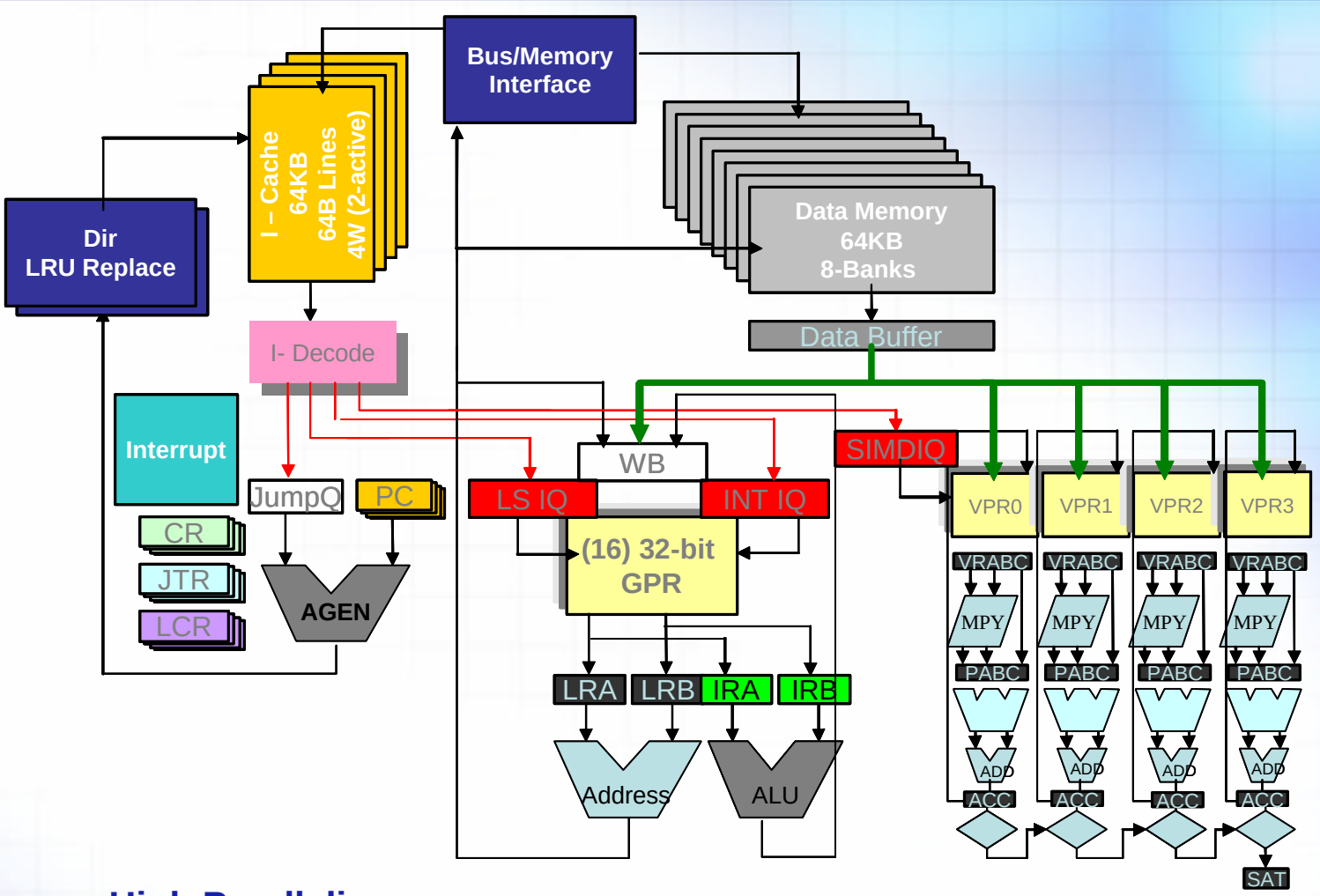
Sandblaster™ Architecture Performs



Multithreaded Baseband Processor



High Parallelism

- Vector / SIMD data parallelism
- Multiple instruction issue
- Thread-level parallelism

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Multithreaded Architecture

Key to Low Power Implementation

Code&Data Sharing Across Threads

Sea of Threads

Hardware Scheduled

Highly Parallel

Fully Interlocked

Fast Cross Thread Interrupts

C Programmed

Thread 0

```
# Monitoring FCCH&SCH
lu  r1,M(r2)
lu  r1,M(r2)
add r2,r3,r4
cmp cf2,r5,r3
jc  cf2,(Synch_off)
```

Thread 1

```
# WCDMA Main
Start Thread0
Start Thread1
Start Thread2

Start Thread13
Start Thread14
loop lc1,0xf0
```

Thread 2

```
# Exit Code   .
 .
Start Thread33
 .
 .
Start Thread24
```

Thread 3

```
# WCDMA Handover Code

ctsr r1,sr2
lu r1,M(r2)
.
jc cf0,(WCDMA_Mode)
```

Thread 4

```
# Pulse shaping Code

lvuvr1,M(r4)
vmacs vr3,vr1,vr2,wr0
loop lcr0,label(4x)
```

Thread 5

```
# FIR Filter

lvu vr1,M(r4)
vmacs
   vr3,vr1,vr2,wr0
loop lcr0,label(4x)
```

Thread 6

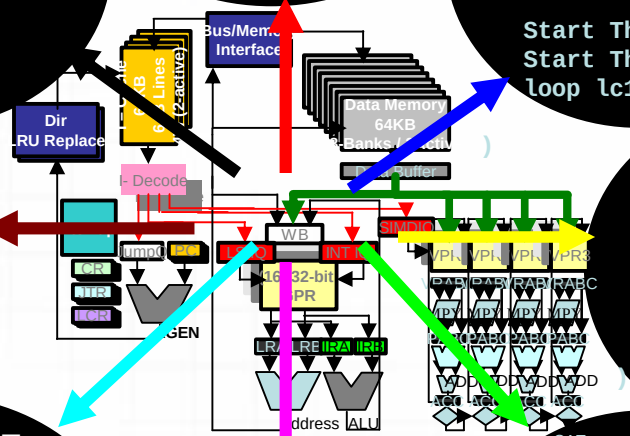
```
# Handover Code

ctsr r1,sr2
lu r1,M(r2)
.
jc cf0,(UMTS_Mode)
```

Thread 7

```
# Monitoring CPICH
lu r1,M(r2)
lu r1,M(r2)
call (De_scrambler)

stu r3,M(r2)
```



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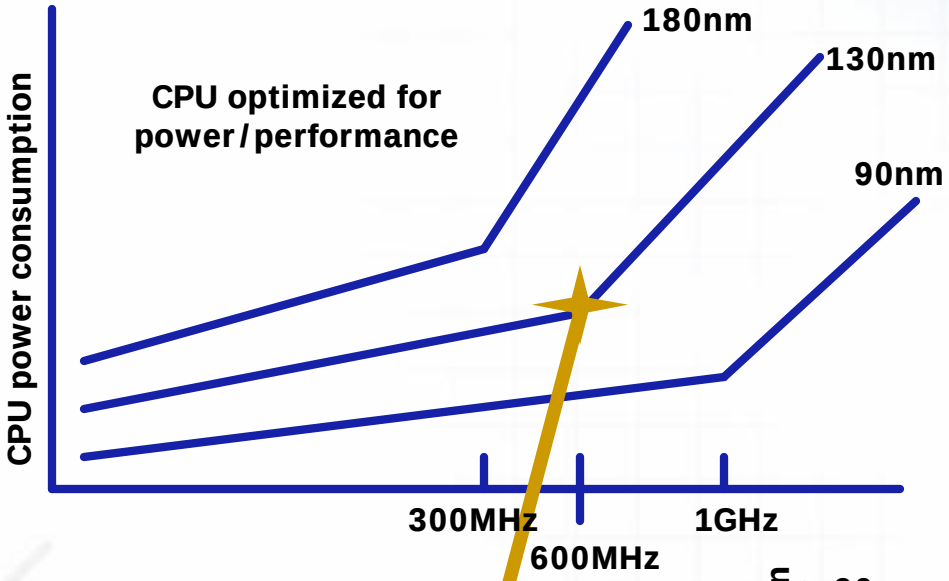
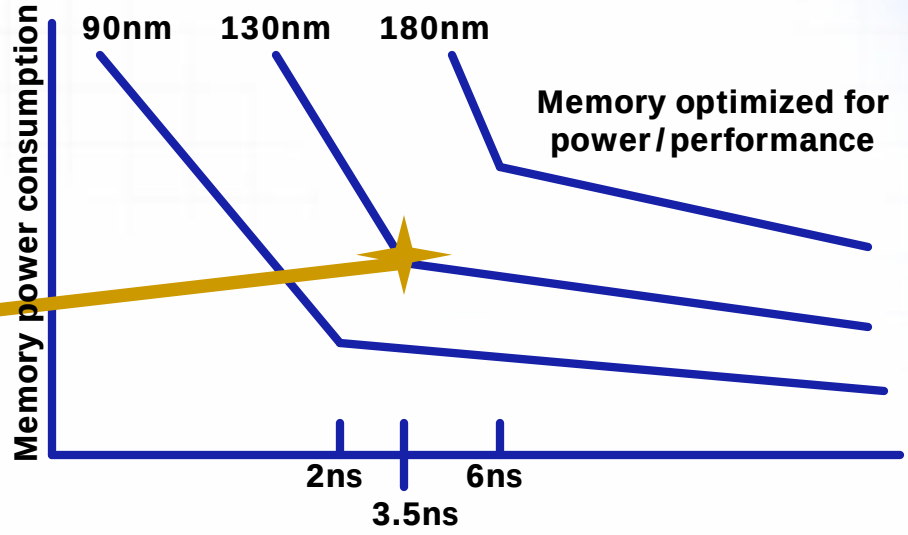
Low power design with No Compromise



Multithreading decouples CPU from Memory speed

Optimized CPU Power

Optimized Memory Power



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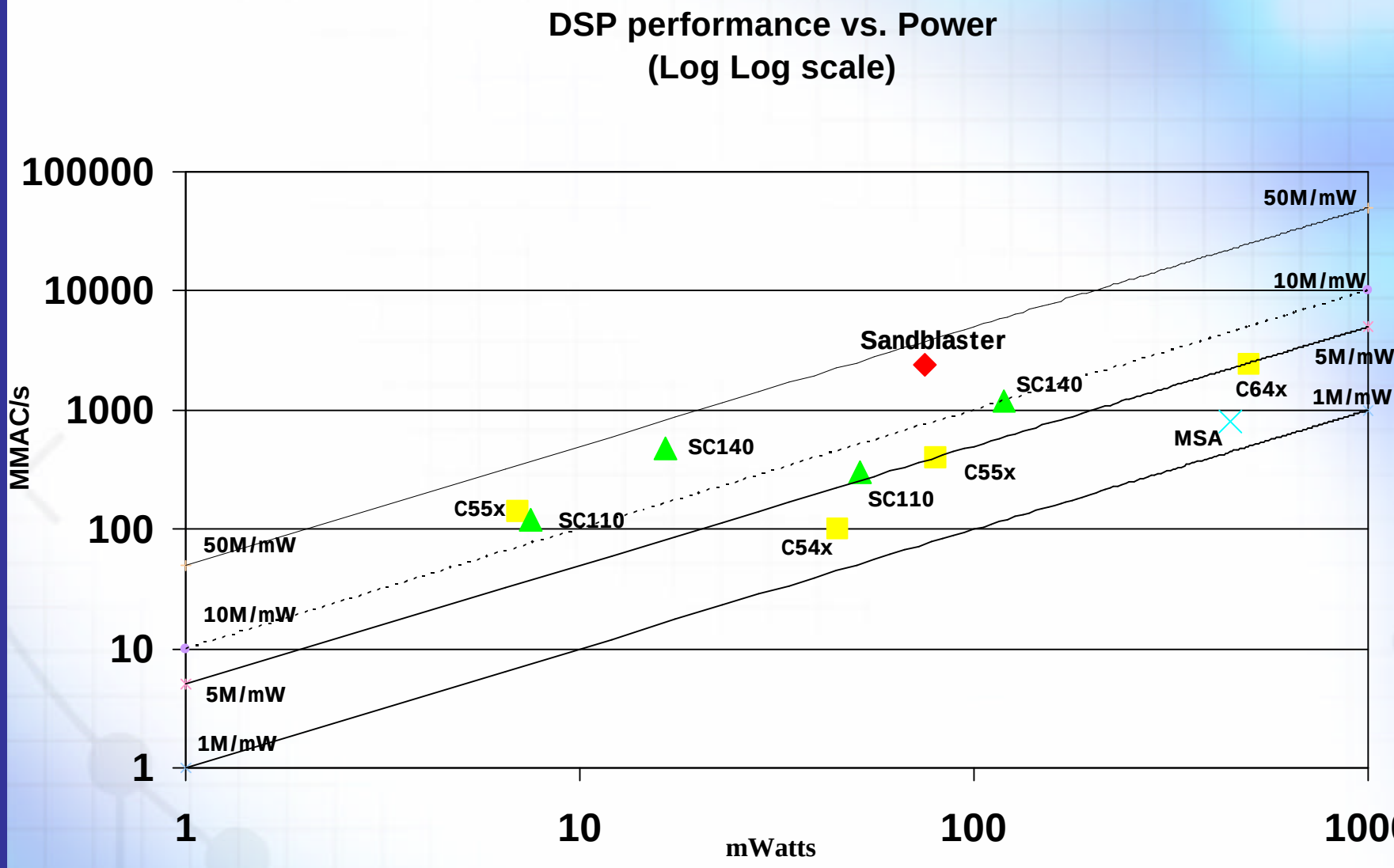
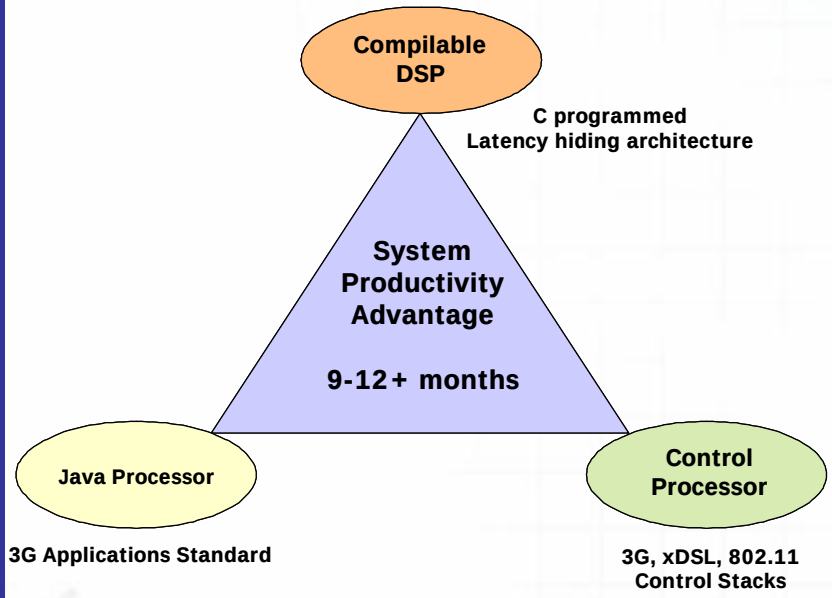
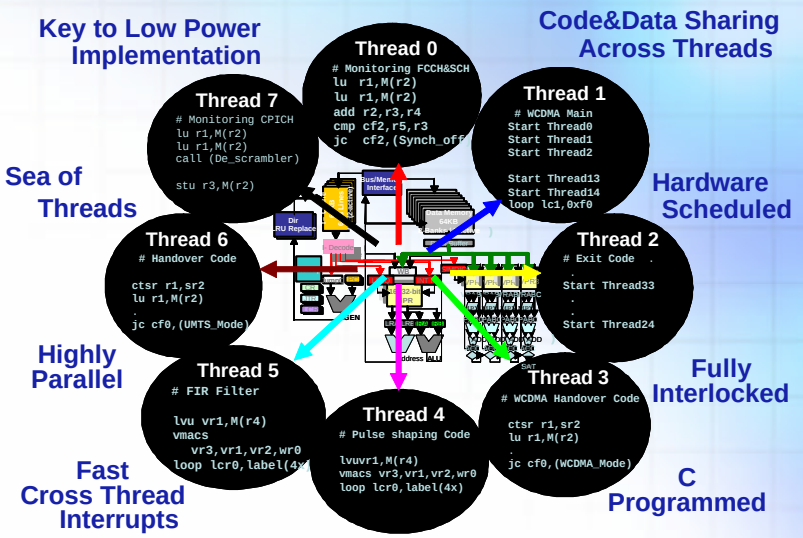
Competitive Power - Cores



… very well received by Industry





MPF Day Two: "Extreme" Processors

Intel's HyperThreading technology looks like child's play compared to SandBridge's new 8-way multithreading capable DSP (digital signal processor) targeted at 3G wireless devices. Replicating and sharing a number of processor resources (that takes about 15% more die area than a hypothetical single-threaded version), up to 8 threads can execute simultaneously in this chip. Apparently, the algorithms and processing steps required for 3G communications can be efficiently allocated across multiple threads and executed simultaneously. The SandBlaster is capable of processing 10 billion multiply/accumulate operations per second, and consumes less than 500 milliwatts on average. Special logic ensures no single thread can dominate the instruction cache, as each thread is only capable of evicting its own specific subset of cache lines. Note that threads can read instruction cache lines from other threads, so that cache is considered to be shared among threads. For power savings, if a thread is not used, it is turned off, and any functional units not presently used can be temporarily powered down.

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Performance

Peak

- 3 compound operations/cycle
- >20 RISC-ops/cycle
- 4 MACS/cycle (MAC-SAT-ADD-SAT)

Example

```
L0: lvu %vr0,%r3,8
||  vmulreds %ac0,%vr0,%vr0,%ac0
||  loop %lc0,L0
```

- >20 operations packed into a 64-bit compound ISA
- VLIW machines may require 512+ bits

20 tap FIR

- 3.63 taps/cycle sustained

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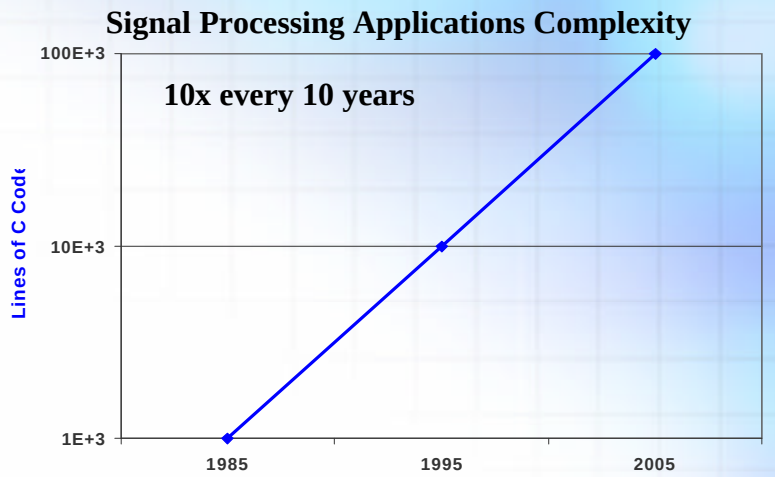
- **Compiler**
- **Simulator**
- **IDE**

Communications System Implementation

- 2Mbps WCDMA
- 802.11b

Compiler Productivity



Design Algorithms

Map to Fixed Point C

Write DSP Specific C

Write DSP Assembly

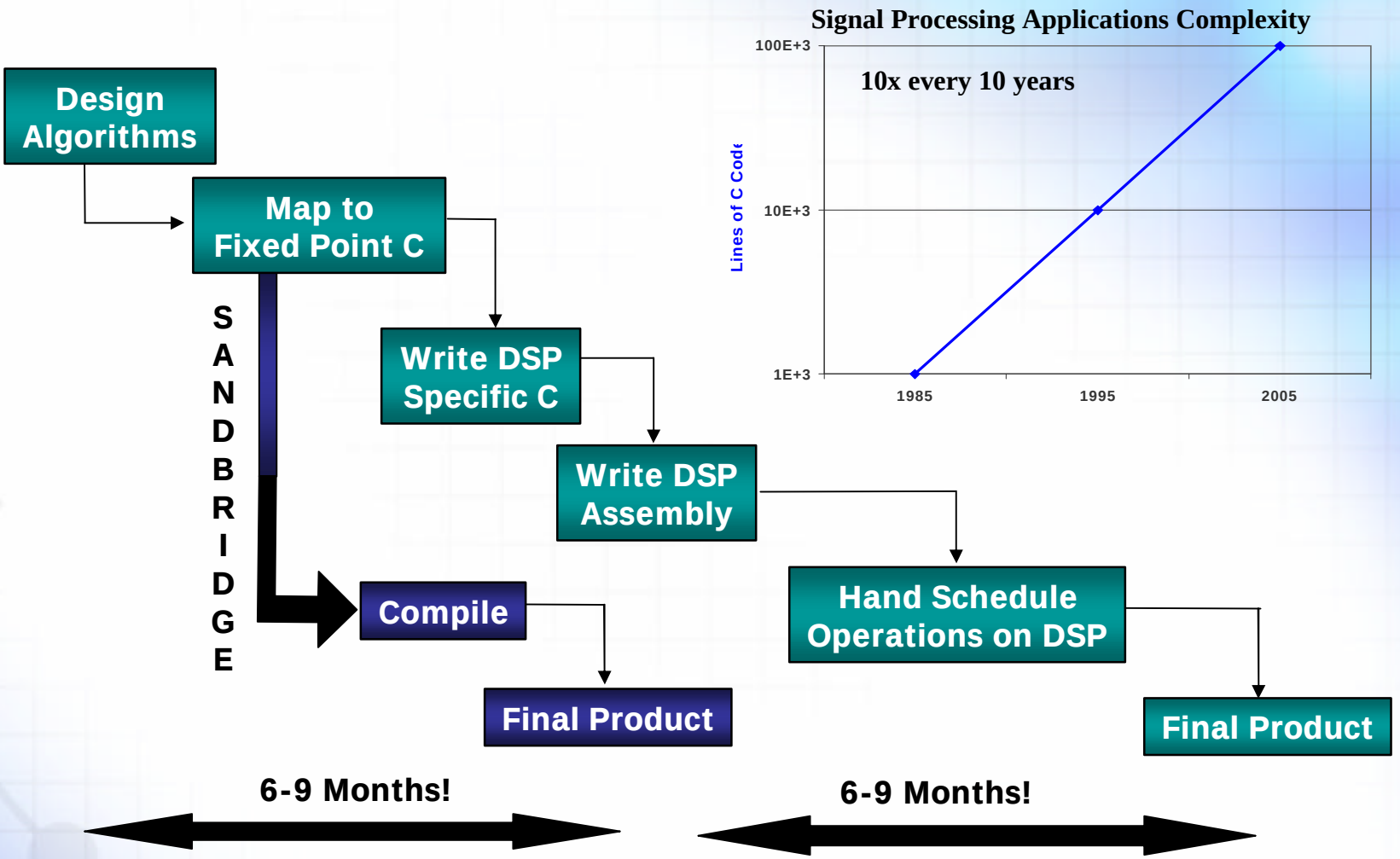
Hand Schedule Operations on DSP

Final Product

6-9 Months!

6-9 Months!

Compiler saves R&D and time-to-market …



Sandblaster™ Provides Dramatic Improvement

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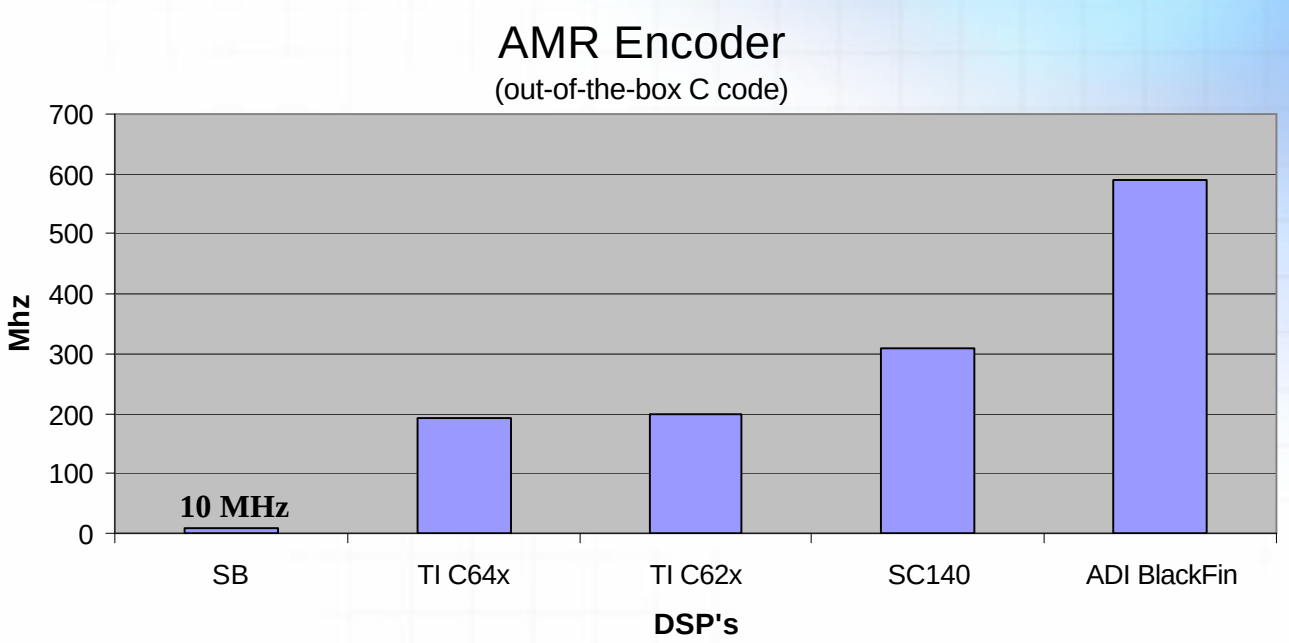
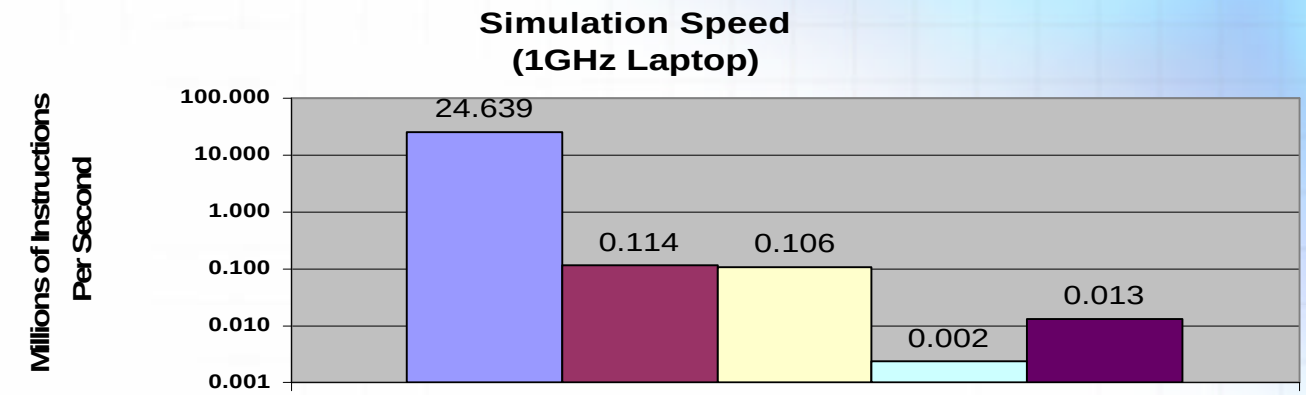
Compiler



Programmed in C or Java

- **Super-computer class compiler**
  - Vectorization
  - DSP instruction generation
- **Standard Library**
  - Printf();
- **POSIX pthreads or Java threads**
- **50k+ testcases used for validation**
  - Industry standards: Plum-Hall, perennial, nullstone

Simulation Software



SB	24.639
TI C64x (Code Composer)	0.114
TI C62x(Code Composer)	0.106
SC140(Metrow erks)	0.002
ADI Blackfin (Visual DSP)	0.013

Compiled Simulator

- JIT “Flash” compilation
- Up to 100 MHz on high end x86
- Multi-threaded supported

Up to 4 orders of magnitude faster

- Dramatic development time reduction
- Significant productivity improvement

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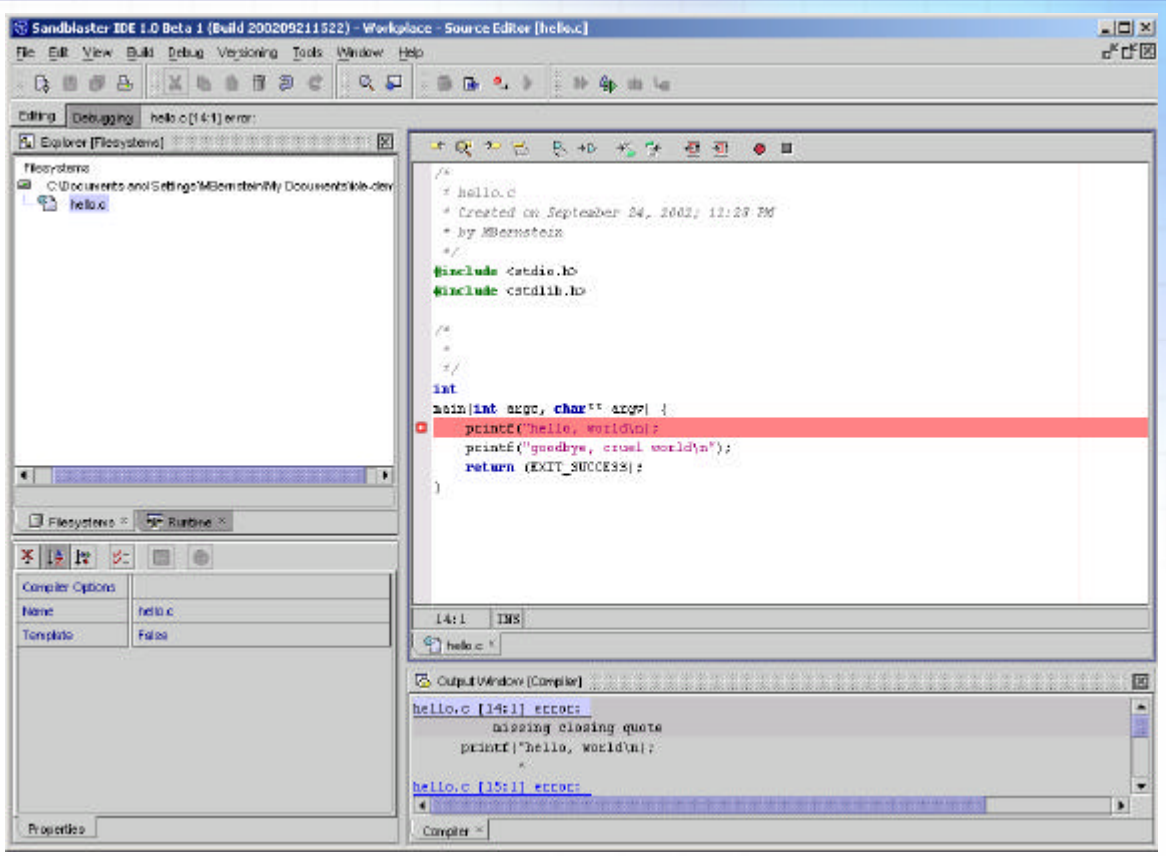
Context sensitive IDE



IDE based on open source netbeans

- Common Java/C programming environment
- Integrated debugging
- Transparent HW / Simulation environment
- Works in multiple languages

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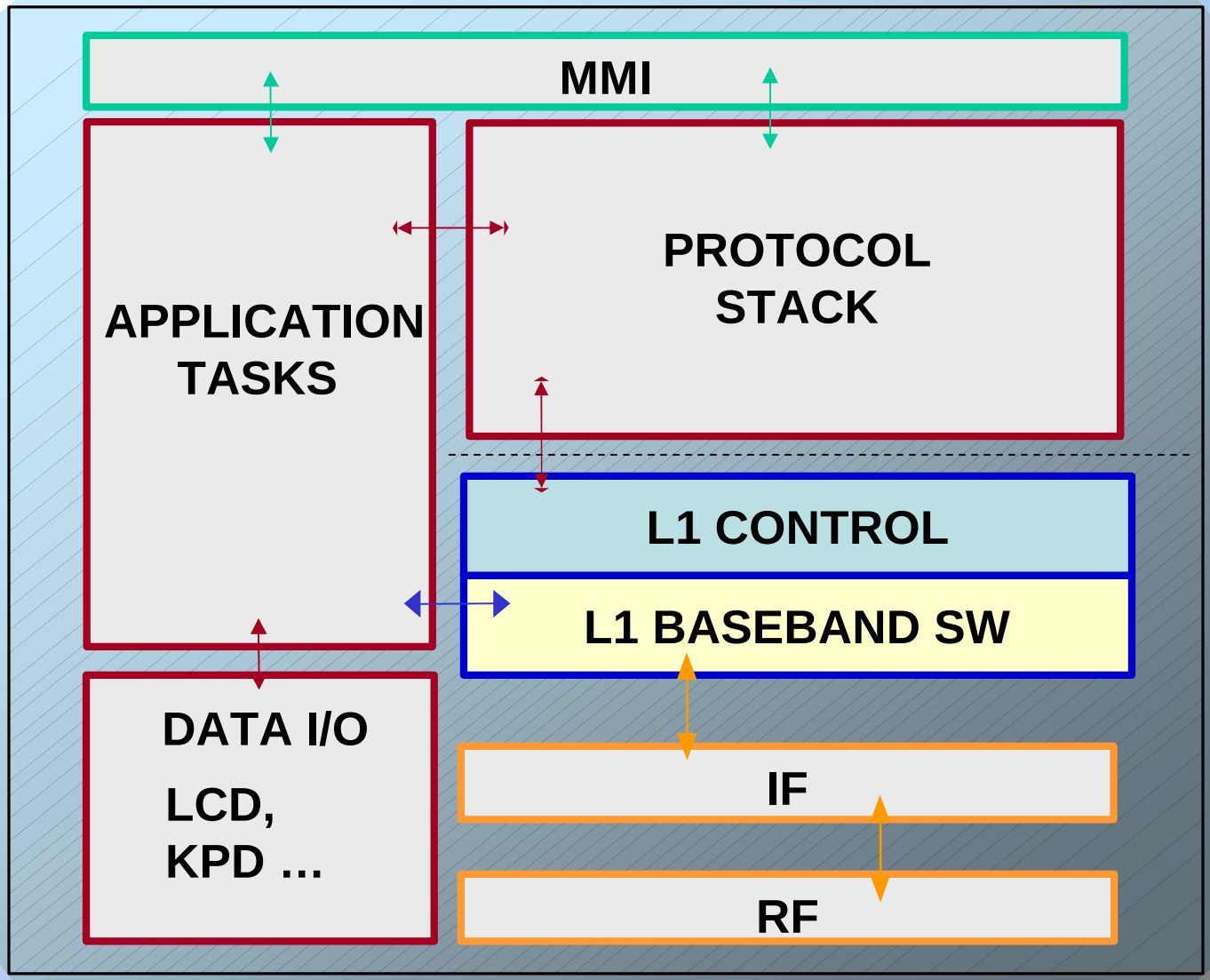
Integration



Application Development Methodology

MATLAB physical layer

- End-to-end UTRAN + UE
- Channel models
- Configurable via test-scripts
- BER/FER measurement

Simulation level C

- Fixed point
- UE only
- Fixed configuration
- Performance measurement

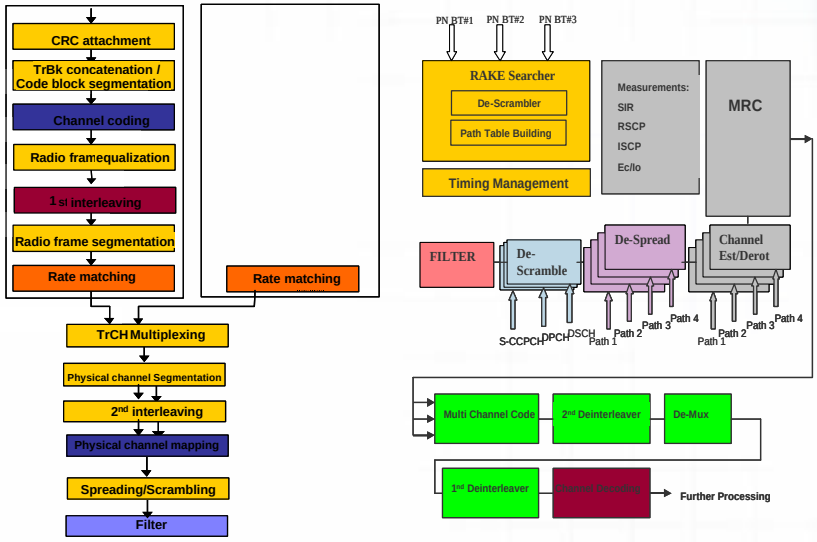
Product level C

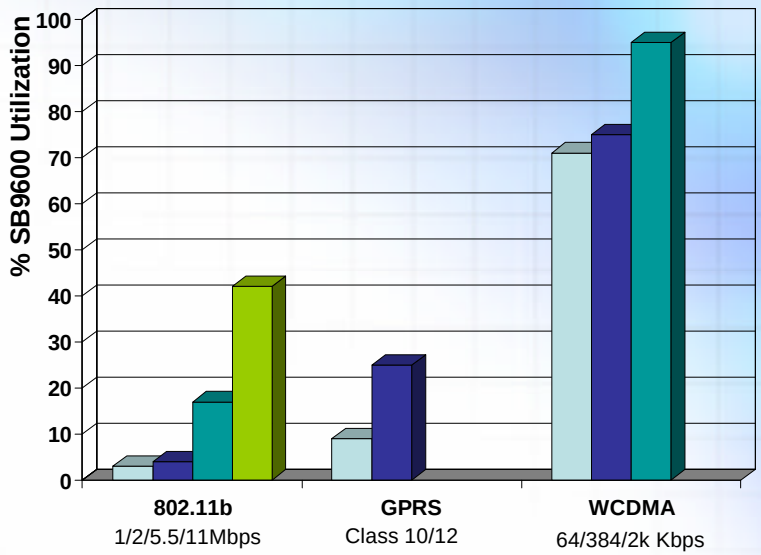
- Partitioned for real-time
- Using actual peripherals
- Integrate with L1 control + L2/L3

Physical layer testing

- UTRAN model validated against test equipment
- models & test cases from 34.121, 25.101, 30.03, ITU

Real-time Baseband Performance





Real-time chip, bit, and symbol rate processing

- 1 SB9600 chip for 2Mbps Rx concurrently with 768kbps Tx
- <75% utilization for 384kbps Rx / 384kbps Tx

Includes functions traditionally implemented in H/W

- Turbo Decoder
- Rake Receiver
- Tx/Rx Filters

Concurrent performance on 802.11B and GPRS

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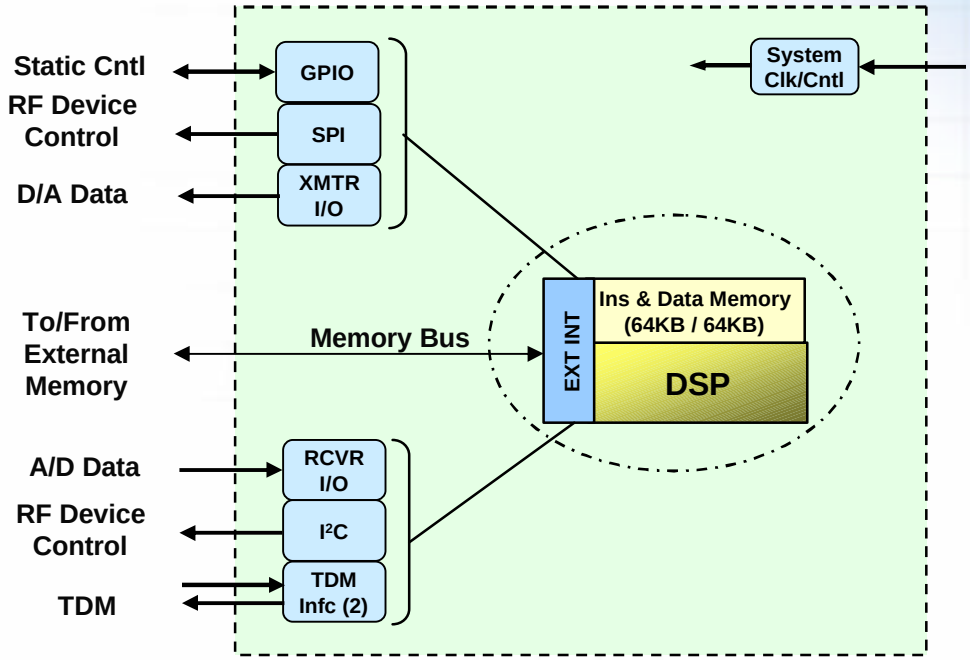
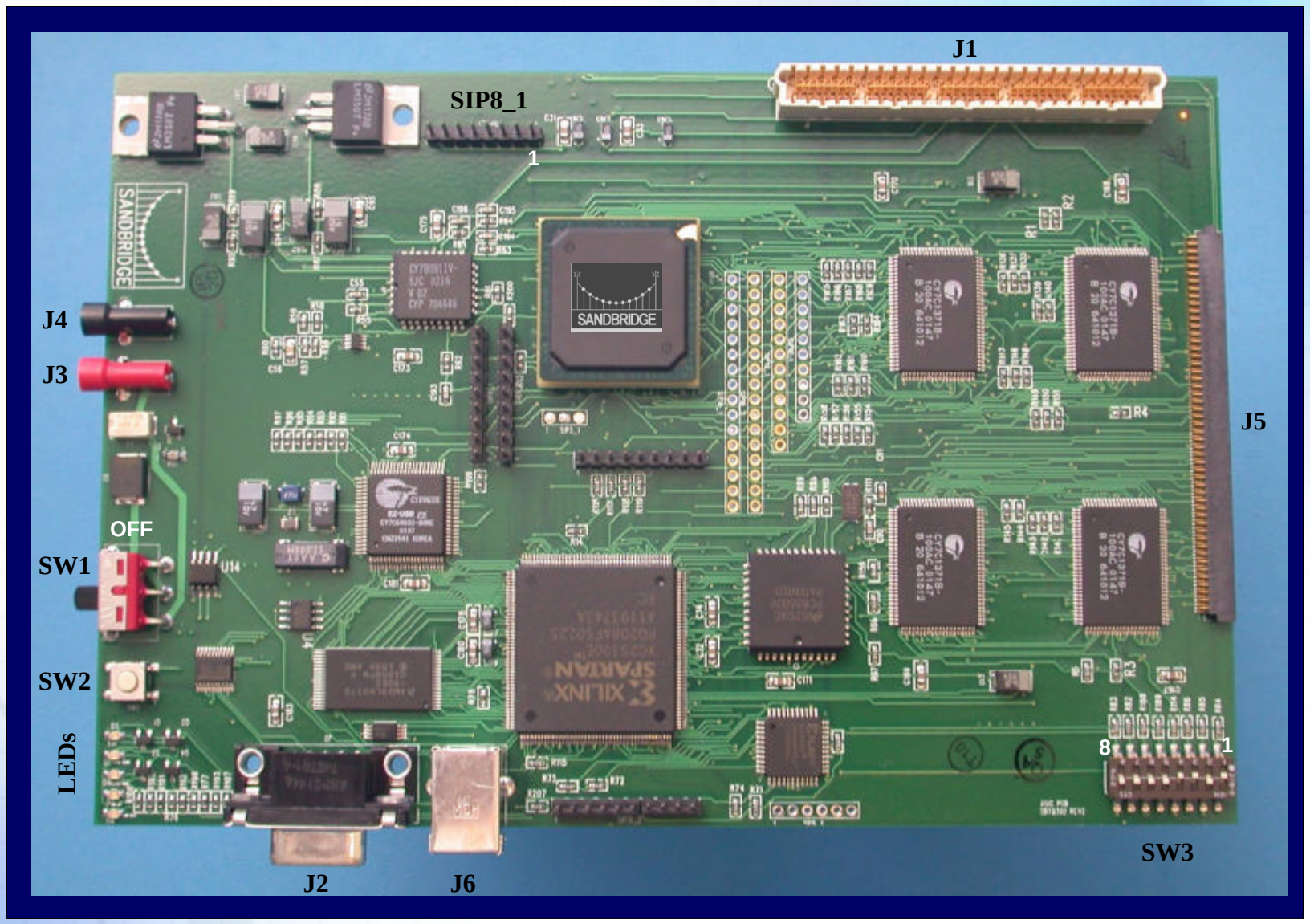
SBTC 8/02

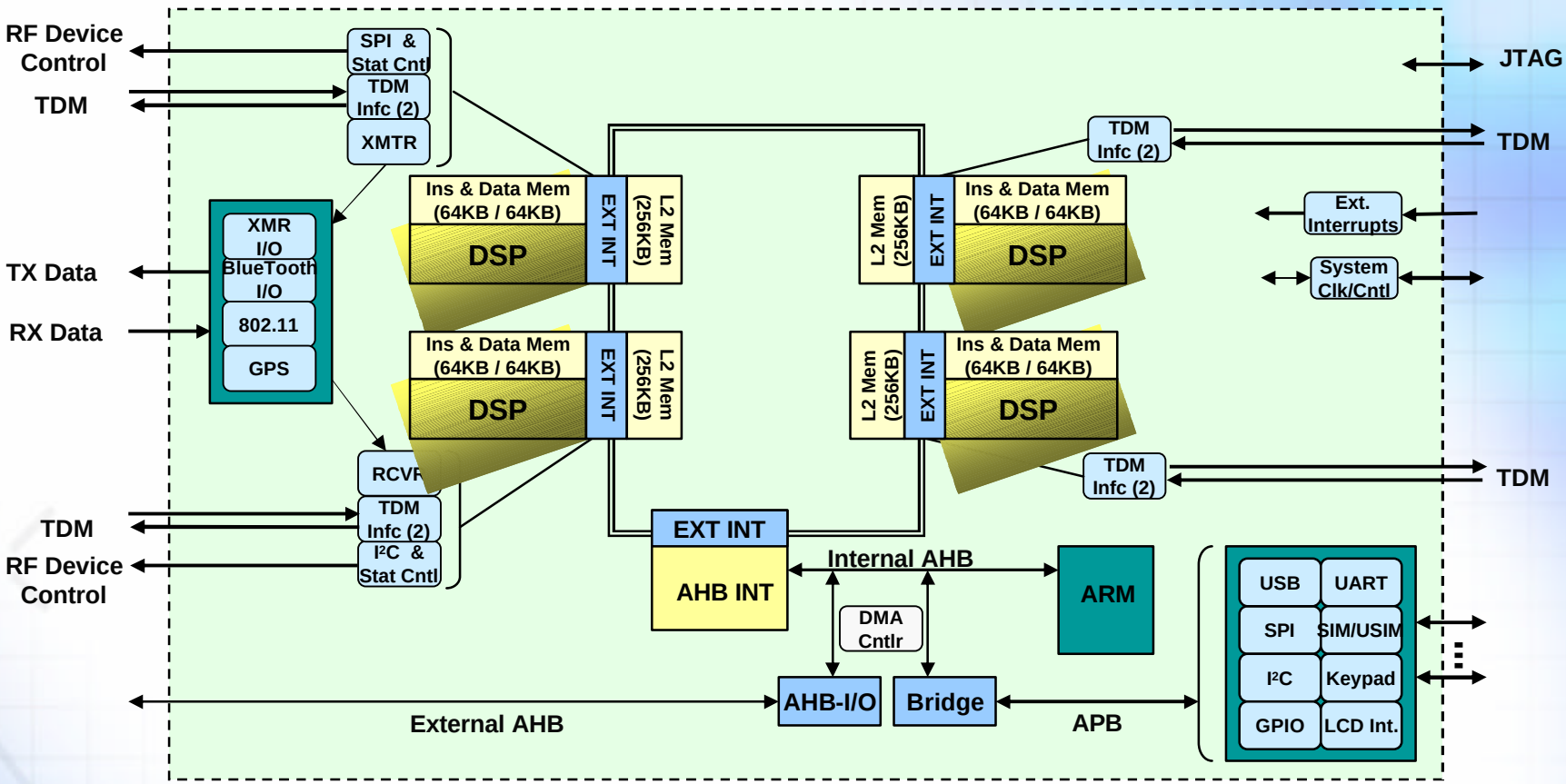


- 0.18um CMOS ASIC
- Single DSP Core
- SW Programmable
- External Bus for L2 memory
- Internal Inst/Data memory
- Control Interfaces: I^2C, SPI, TDM, A/D, D/A

Populated Multimode Baseband Card



SB9600 2003 Handset Chip



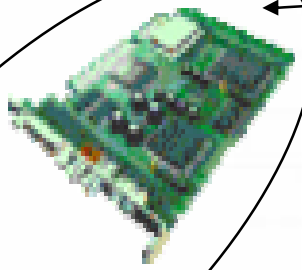
- 0.13um CMOS, *custom*
- Replicated SBTC core
- Low Power design

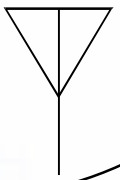
Capabilities

End use integration

Design Integration Capability

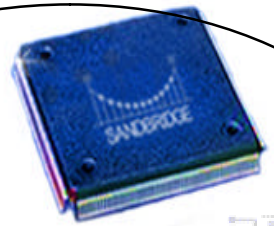
- RF Integration
- Card Design

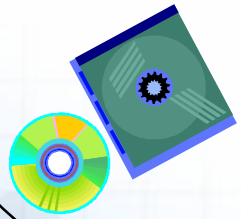


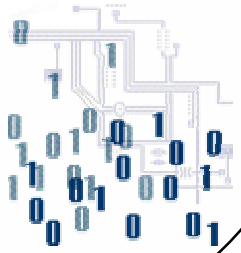


Key Sandbridge Expertise

- Software Systems
  - Compilers
  - Compiled Simulators
- Computer Architecture
  - DSP / Processor Design
  - Java Execution
- Wireless Communications
  - Transmission Systems Algorithm Design
  - 3G
- Low Power VLSI Design







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Summary

Multithreaded baseband processor

- High-performance and low-power
- DSP, Java, and Control processing

Sophisticated compiler technology

- Automatically generates DSP operations
- Automatically multithreads applications
- Hand coded performance

Reconfigurable Communications Protocols

- WCDMA, GSM, GPRS, etc.
- 802.11b, Bluetooth, etc.

Multimedia capability

- MP3
- MPEG4