



# Wireless SDR Solutions: The Challenge and Promise of Next Generation Handsets

**John Glossner, Ph.D., Founder, CTO & EVP**

**Erdem Hokenek, Ph.D., Founder, Chief H/W Architect**

**Mayan Moudgill, Ph.D., Founder, Chief S/W Architect**

[glossner@SandbridgeTech.com](mailto:glossner@SandbridgeTech.com)

1 North Lexington Ave, 10<sup>th</sup> Floor

White Plains, New York 10601

914-287-8500

# Agenda

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**Motivation for SDR**

**Market**

**Technology Requirements**

**Sandbridge Technologies' Solution**

# Agenda

## Motivation for SDR

Market

Technology Requirements

Sandbridge Technologies' Solution

# The Challenges of an Industry

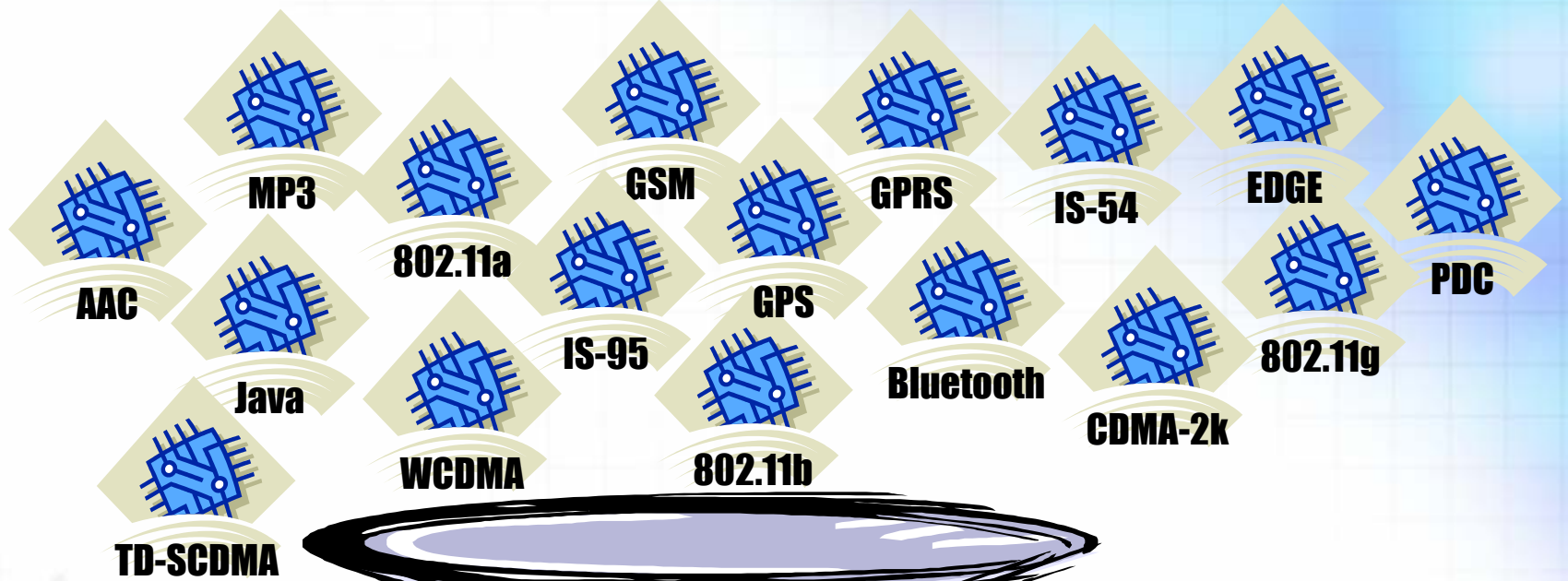
## Cost

- ➔ **3G is >10x more complex than 2G**
  - but cost should be same, or even less
- ➔ **Convergence phone 2x complexity**
  - WLAN, 2G, and 2.5G integration
  - Traditionally implemented in HW
- ➔ **Moore's law reduces cost 50% every 18 months**
  - 6 years until the wireless multimedia is a real consumer market

## Time-to-market

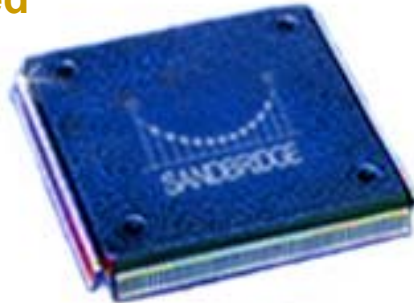
- ➔ **GPRS terminals were late**
  - OEMs had to wait until bug free SoCs were available
- ➔ **3G terminals will be late**
  - OEMs have to wait until bug free SoCs with 'reasonable' power consumption are available

# Multifunction Devices



Software Defined,  
Sandblaster™ Mastered

Sandbridge's reconfigurable  
baseband technology  
minimizes silicon  
requirements and optimizes  
flexibility



# Agenda

Motivation for SDR

**Market**

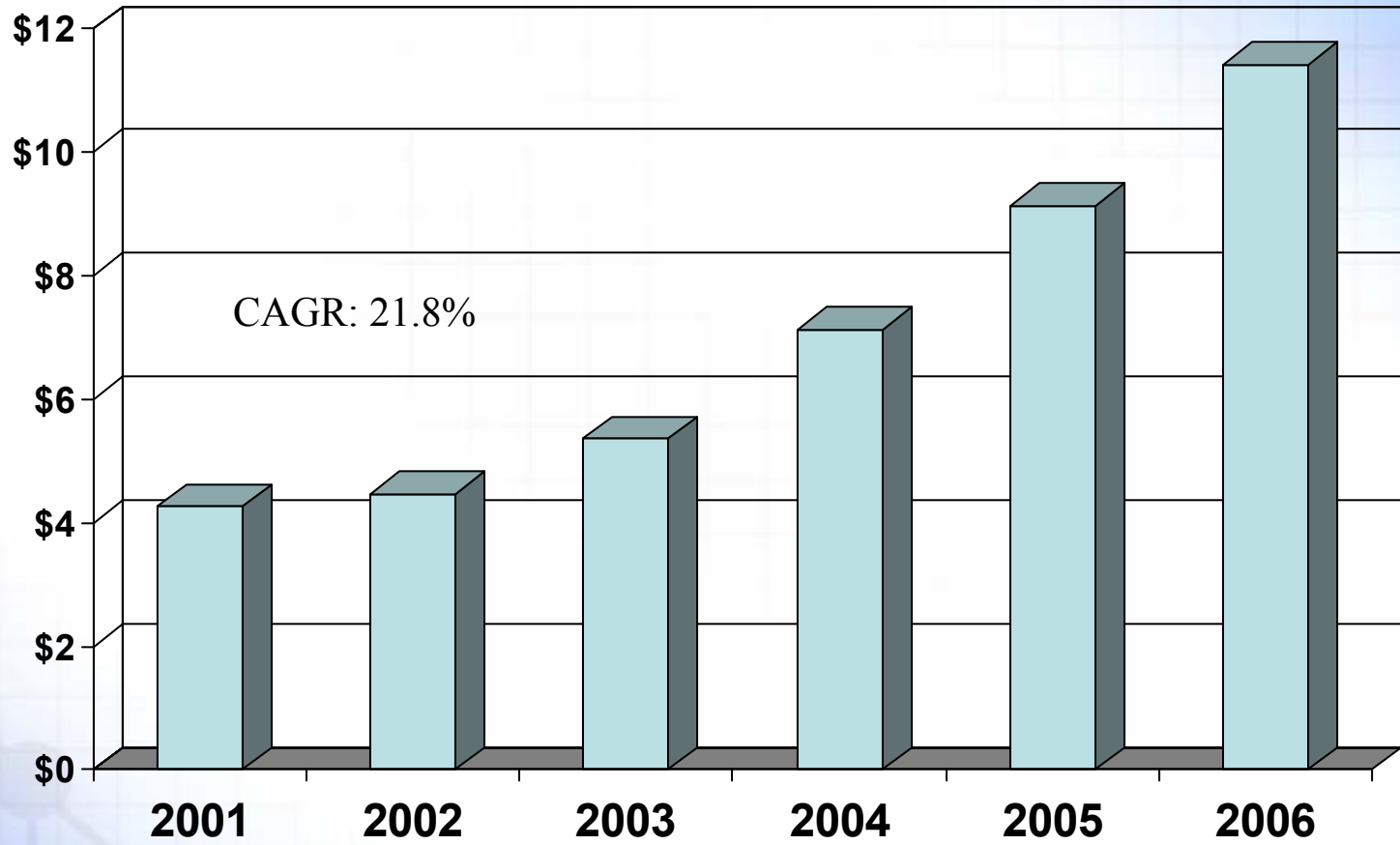
Technology Requirements

Sandbridge Technologies' Solution

# Programmable DSP Market

## Programmable DSP Market

Billions



Source: Forward Concepts 2002

# Agenda

Motivation for SDR

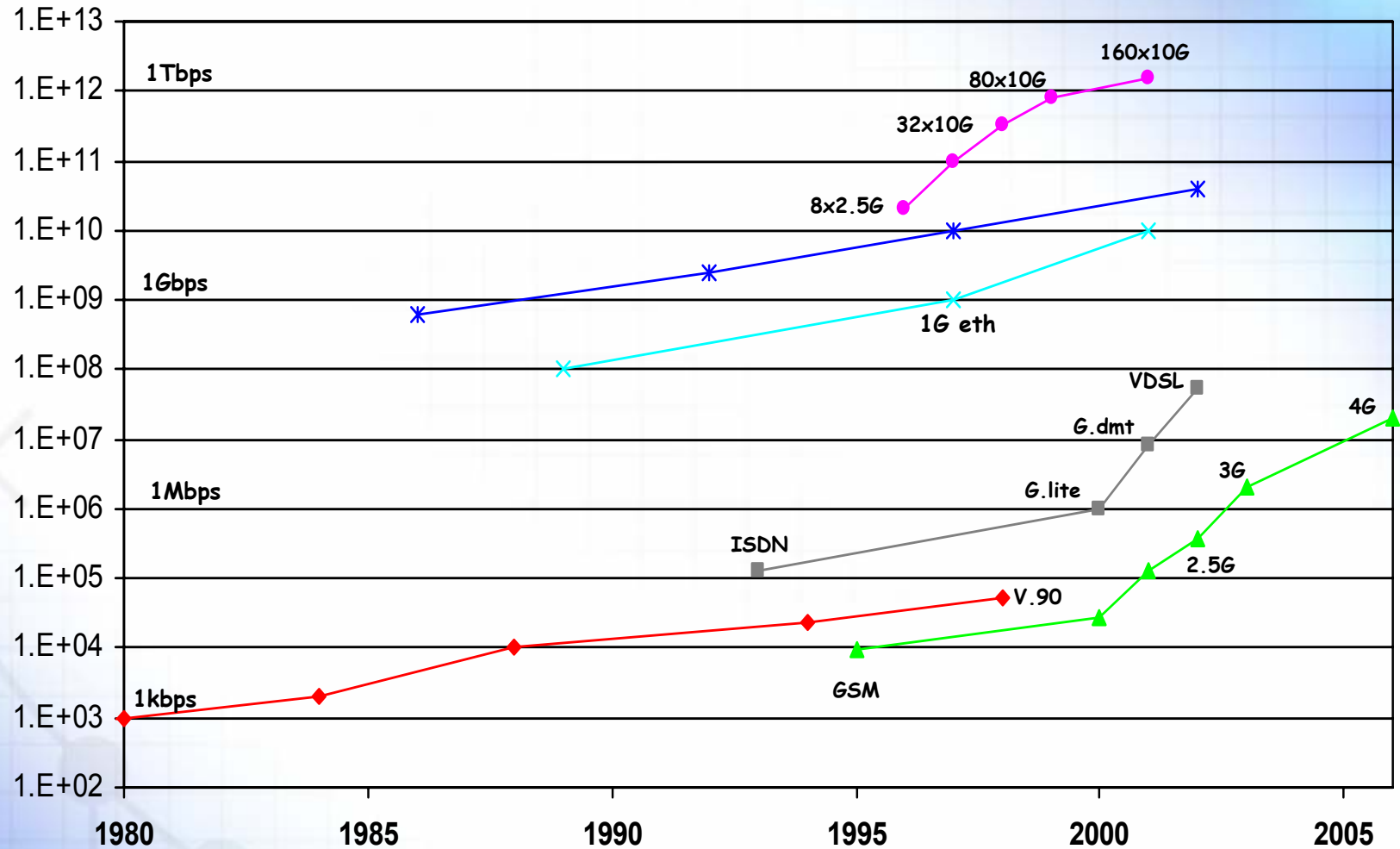
Market

**Technology Requirements**

Sandbridge Technologies' Solution

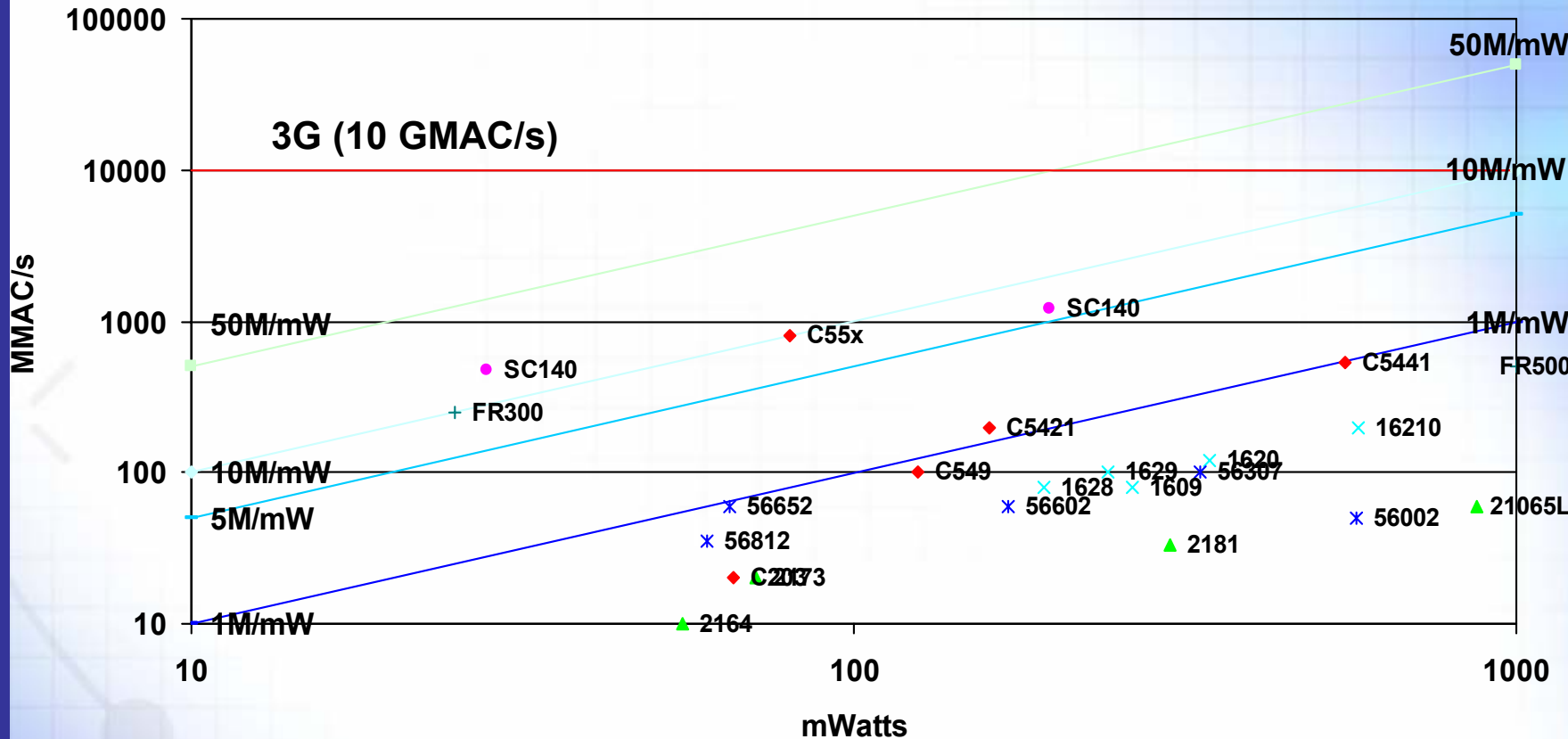


# Datarate Evolution



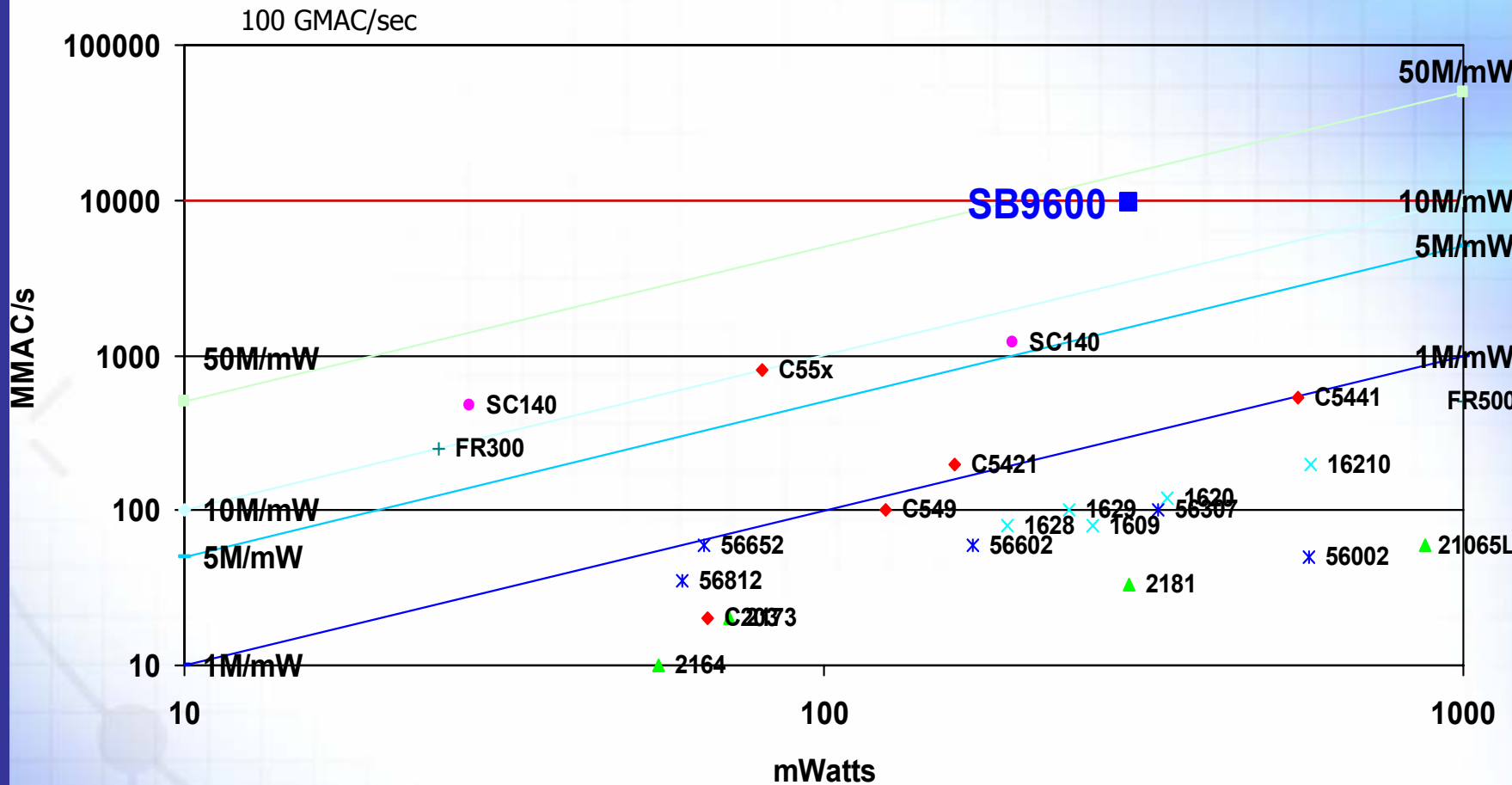
# DSP Power/Performance

DSP Performance vs. Power  
(Log Log scale)



# Competitive Power

## DSP Performance vs. Power (Log Log scale)



# Agenda

Motivation for SDR

Market

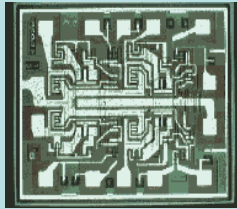
Technology Requirements

**Sandbridge Technologies' Solution**

# Sandbridge Approach

Available now

## SandBlaster™ DSP



- Programmable
- Ultra-low power
- High-performance
- Multithreaded

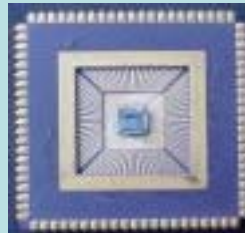
## SandBlaster™ Tools



- High productivity C compiler
- 70% time-to-market reduction
- User-friendly Environment

Q3-03

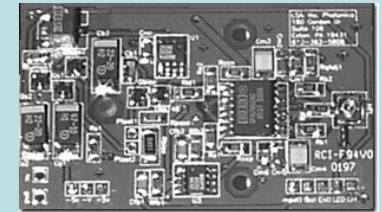
## SB9600 Baseband



- Scalable & Programmable
- Integrated Sandblaster cores
- Up to 2Mbit/sec data rate
- 40,000 RISC MIPS
- 10,000 MMACs
- Low Cost 0.13um CMOS
- Integrated protocol stack

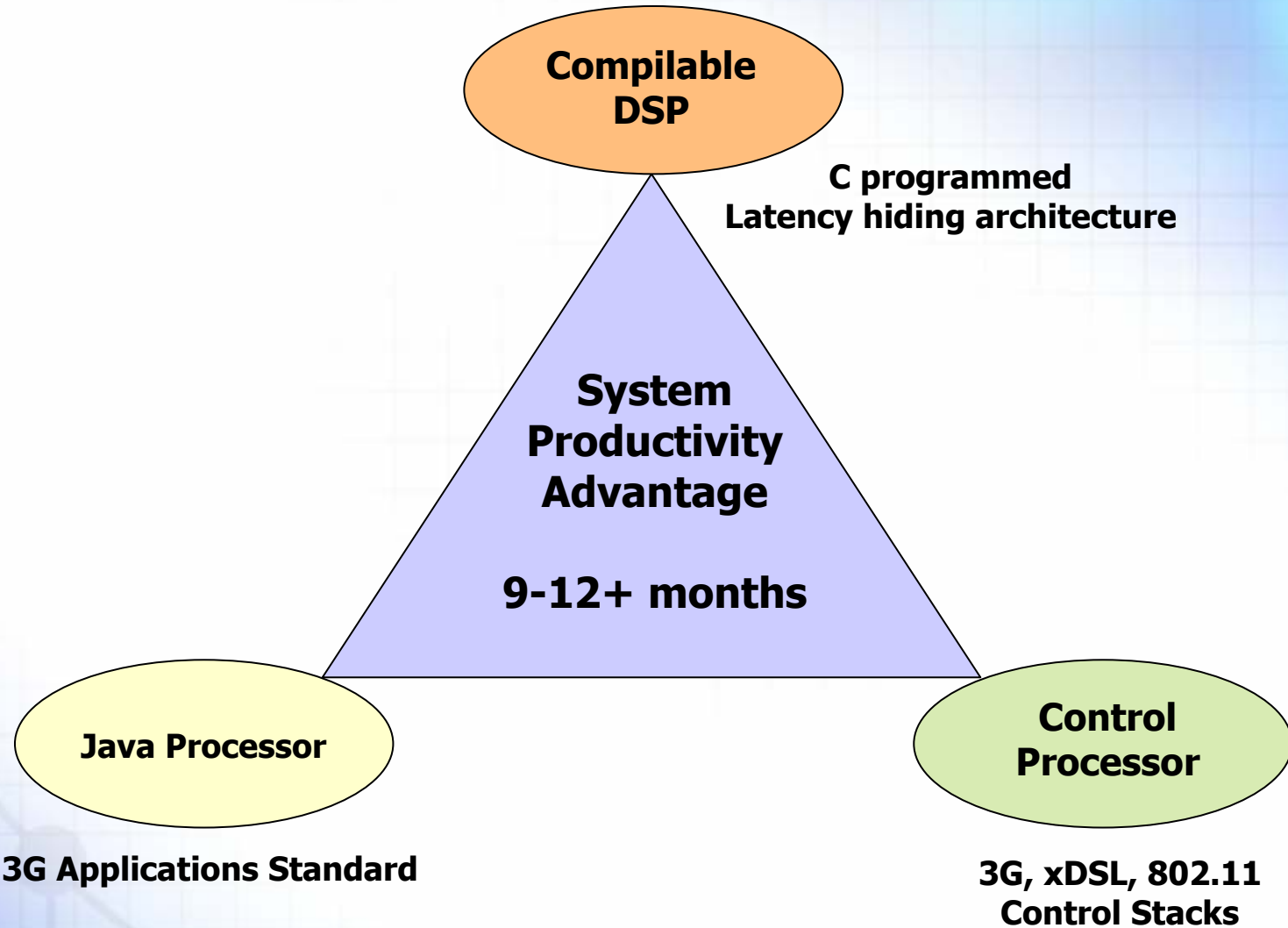
Q1-04

## Multi-function System Solution

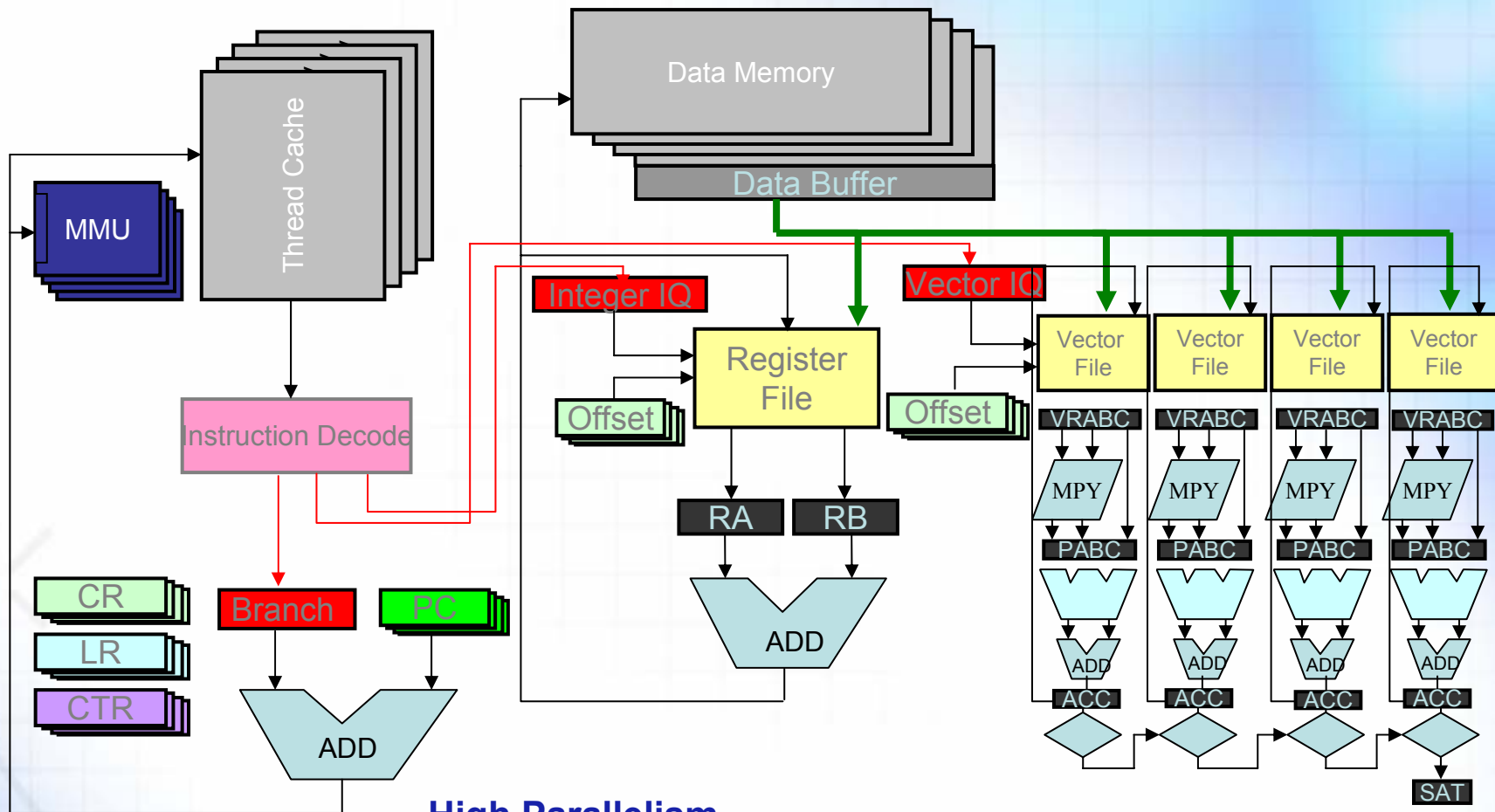


- Low Cost
- Power Efficient
- Ultra-high performance
- Fully tested / validated
- Dedicated Customer Support
- Flexible and upgradeable

# Sandblaster™ Architecture Performs



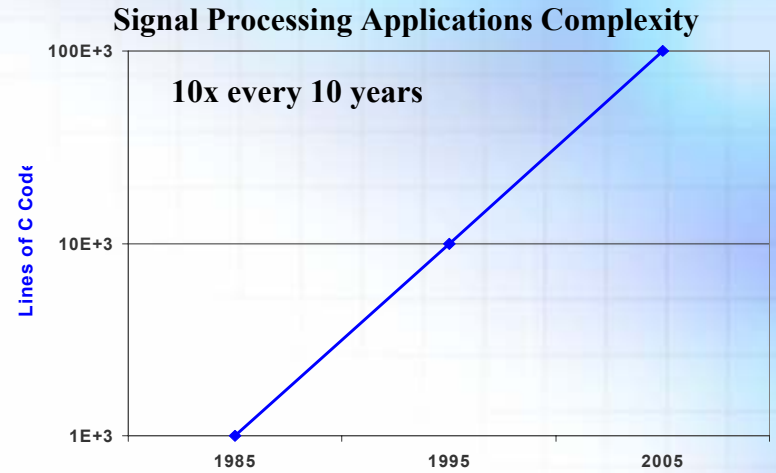
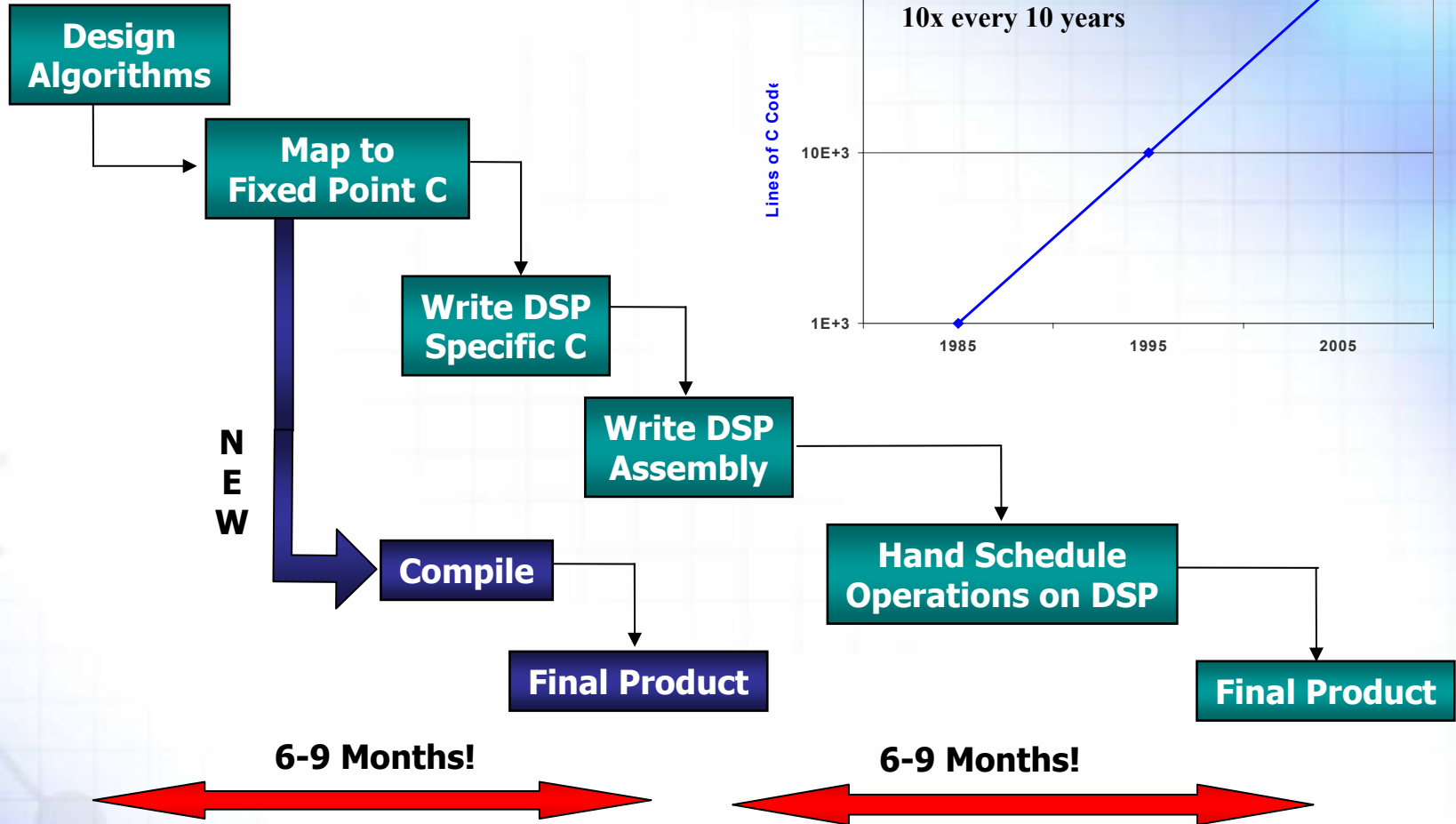
# Multithreaded DSP



## High Parallelism

- Vector / SIMD data parallelism
- Multiple instruction issue
- Thread-level parallelism

# Compiler Productivity



**Sandblaster™ Provides Dramatic Improvement**



# Compiler Optimizations

## DSP Optimizations

Saturation Arithmetic  
Fixed Point Semantic Analysis  
Bit-exact ETSI compliance

## Vector Optimizations

Vector Loads  
Vector Stores  
Vector Arithmetic  
Vector Reduction  
Saturating Vector Operations

## Loop Optimizations

Loop Invariant Code Motion  
Strength Reduction  
Induction Variable Elimination  
Loop Splitting  
Software Pipelining

## Scalar Optimizations

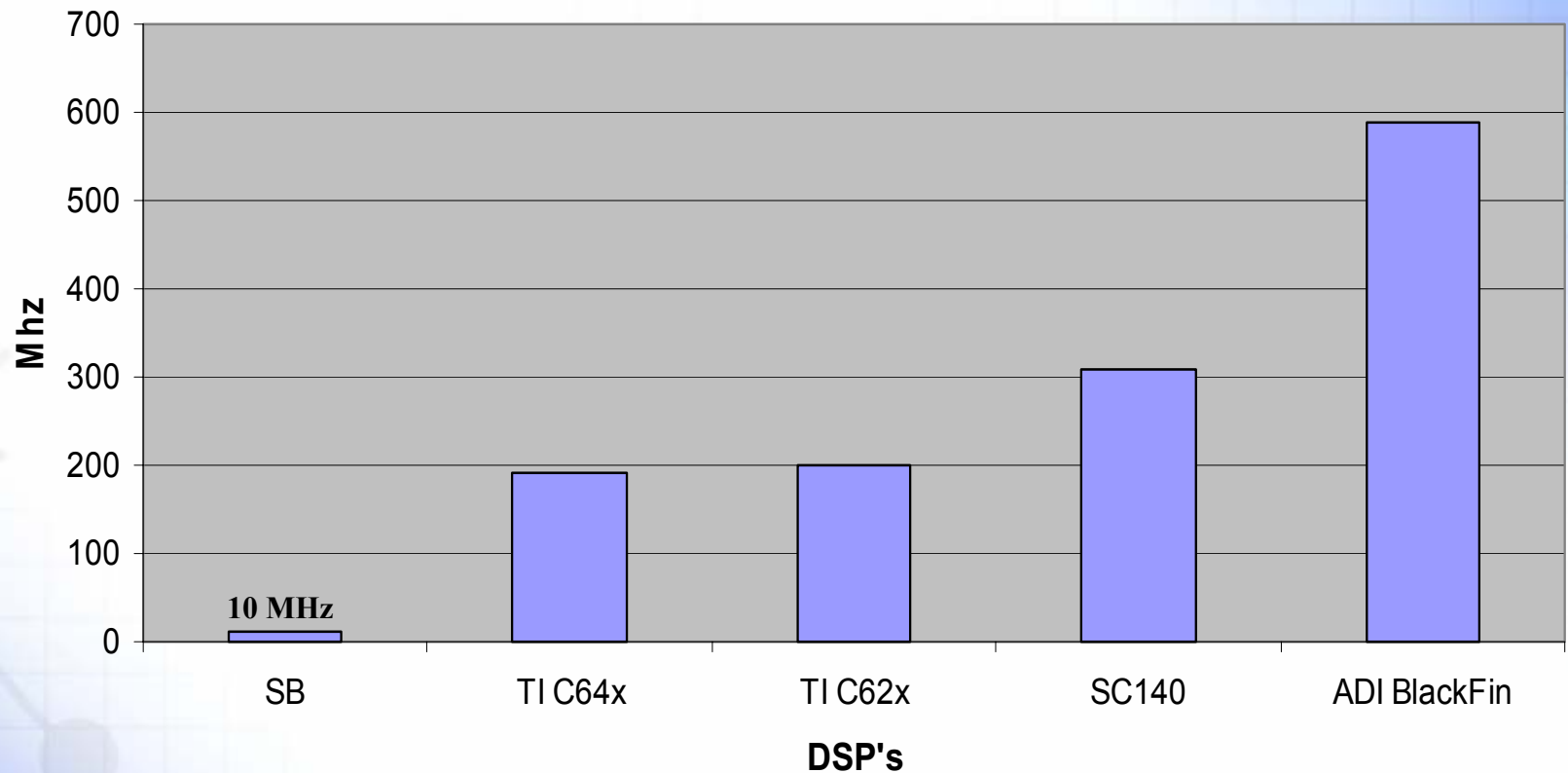
Range/type Propagation  
Common Subexpression Elim.  
Constant Folding  
Dead Code Elimination  
Register Coloring

## Interprocedural Opts.

Constant Propagation  
Memory Disambiguation  
Function Inlining  
Alias Analysis

# AMR Out of Box Results

## AMR Encoder



# Simulation Technology

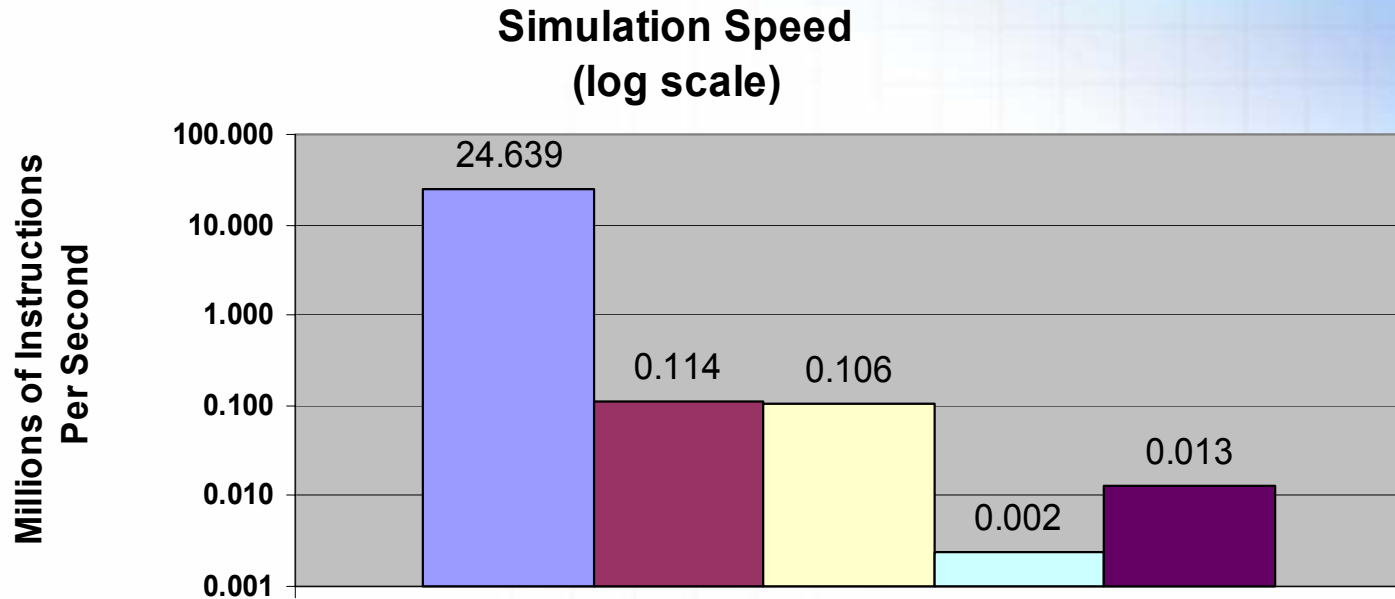
## Compiled Simulator

- ➔ 100 MHz on high end x86
- ➔ JIT “Flash” compilation
- ➔ Multi-threaded supported
- ➔ Function level profiler
  - Non-intrusive
- ➔ Up to 4 orders of magnitude faster
  - Dramatic development time reduction
  - Significant productivity improvement

## Cycle Accurate Simulator

- ➔ Used for Verification against VHDL model
- ➔ Provides detailed statistics

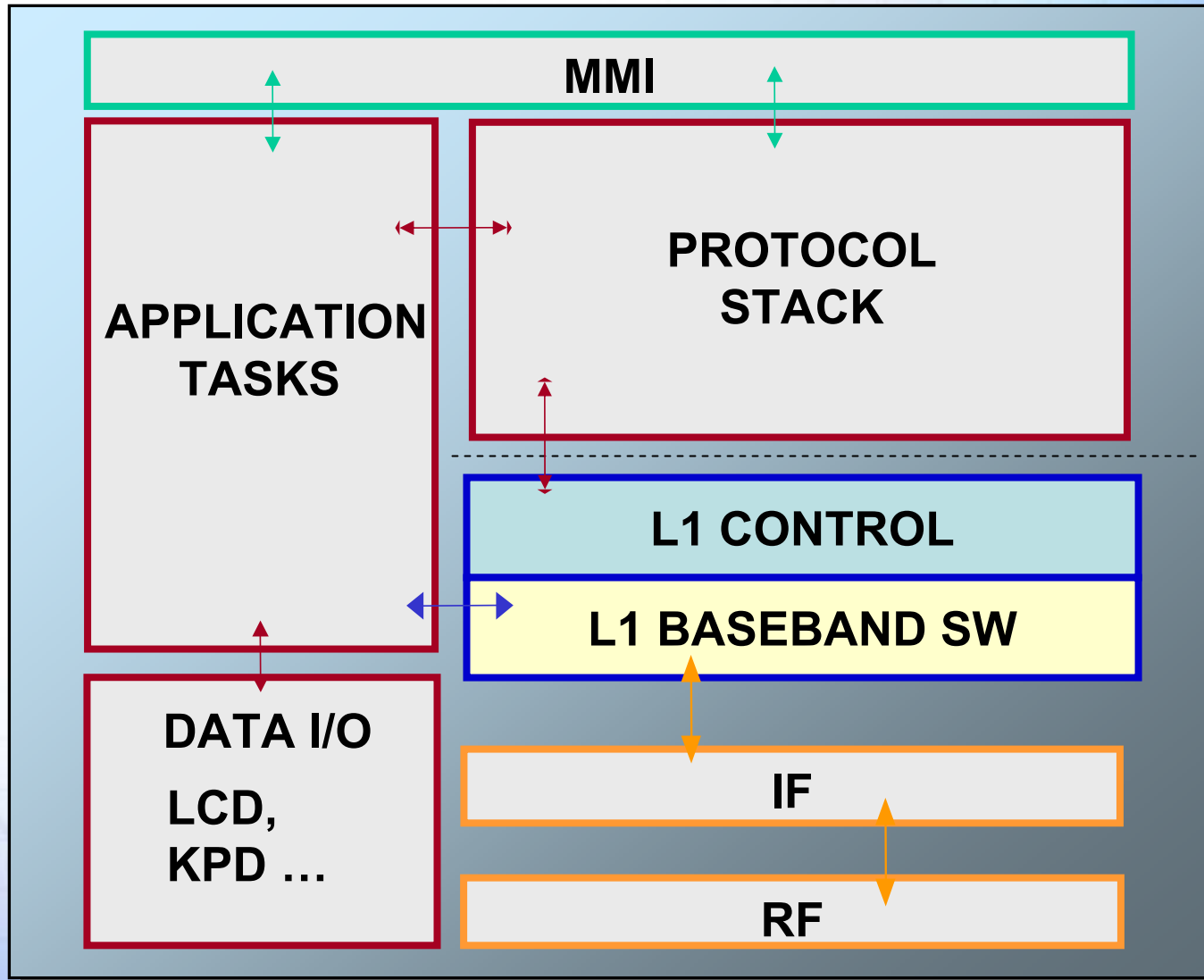
# Functional Simulator Speeds



■ SB	24.639
■ TI C64x (Code Composer)	0.114
■ TI C62x (Code Composer)	0.106
■ SC140 (Metrowerks)	0.002
■ ADI Blackfin (Visual DSP)	0.013

**Results on 1Ghz laptop**

# Integration



# Development Process

## MATLAB physical layer

- ➔ End-to-end UTRAN + UE
- ➔ Channel models
- ➔ Configurable via test-scripts
- ➔ BER/FER measurement

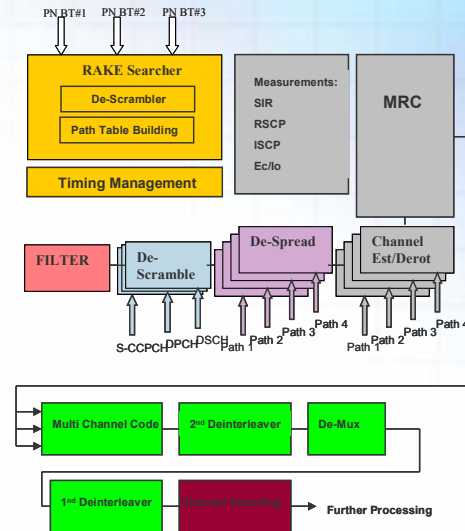
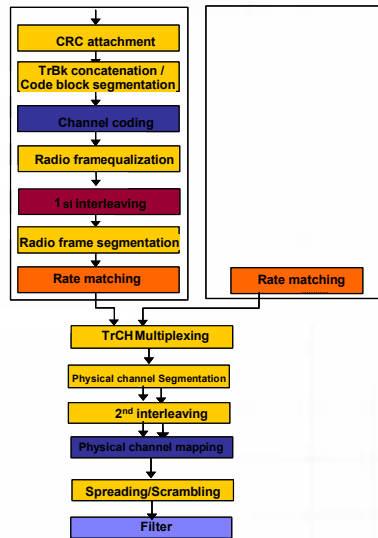
## Product level C

- ➔ Partitioned for real-time
- ➔ Using actual peripherals
- ➔ Integrate with L1 control + L2/L3

## Simulation level C

- ➔ Fixed point
- ➔ UE only
- ➔ Fixed configuration
- ➔ Performance measurement

# Real-time WCDMA Performance



## Real-time chip, bit, and symbol rate processing

- 1 SB9600 chip for 2Mbps Rx concurrently with 768kbps Tx
- <75% utilization for 384kbps Rx / 384kbps Tx

## Includes functions traditionally implemented in H/W

- Turbo Decoder
- Rake Receiver
- Tx/Rx Filters

# SB9600 Features

## Communications Protocols

- ➔ GSM / GPRS / WCDMA multimode
- ➔ Bluetooth / GPS / 802.11b

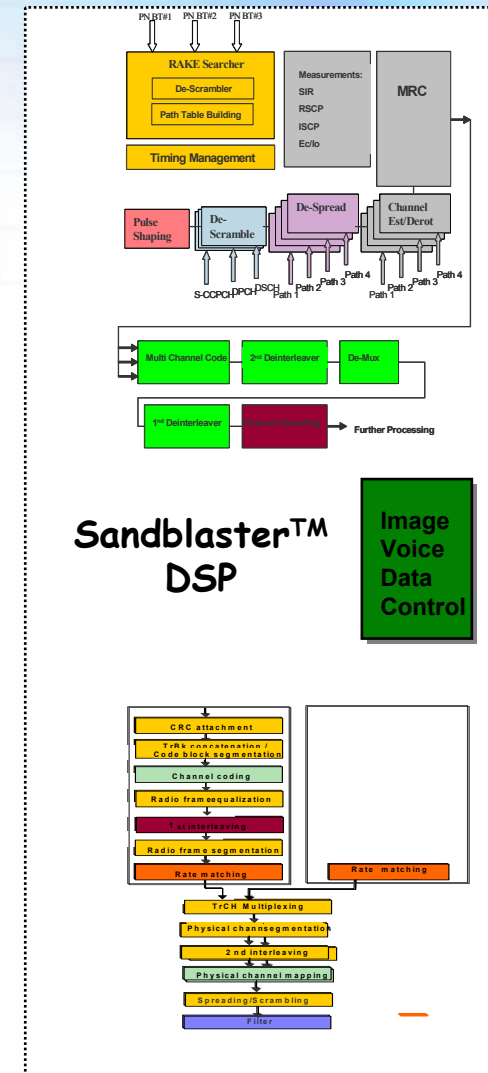
## Audio/Video/Telephony

- ➔ MP-3 / AAC / MIDI / WMA / Real
- ➔ MPEG-4 (QCIF, 15fps)
- ➔ VoIP (H.263, G.723.1)
- ➔ Still & Video Camera

## Misc

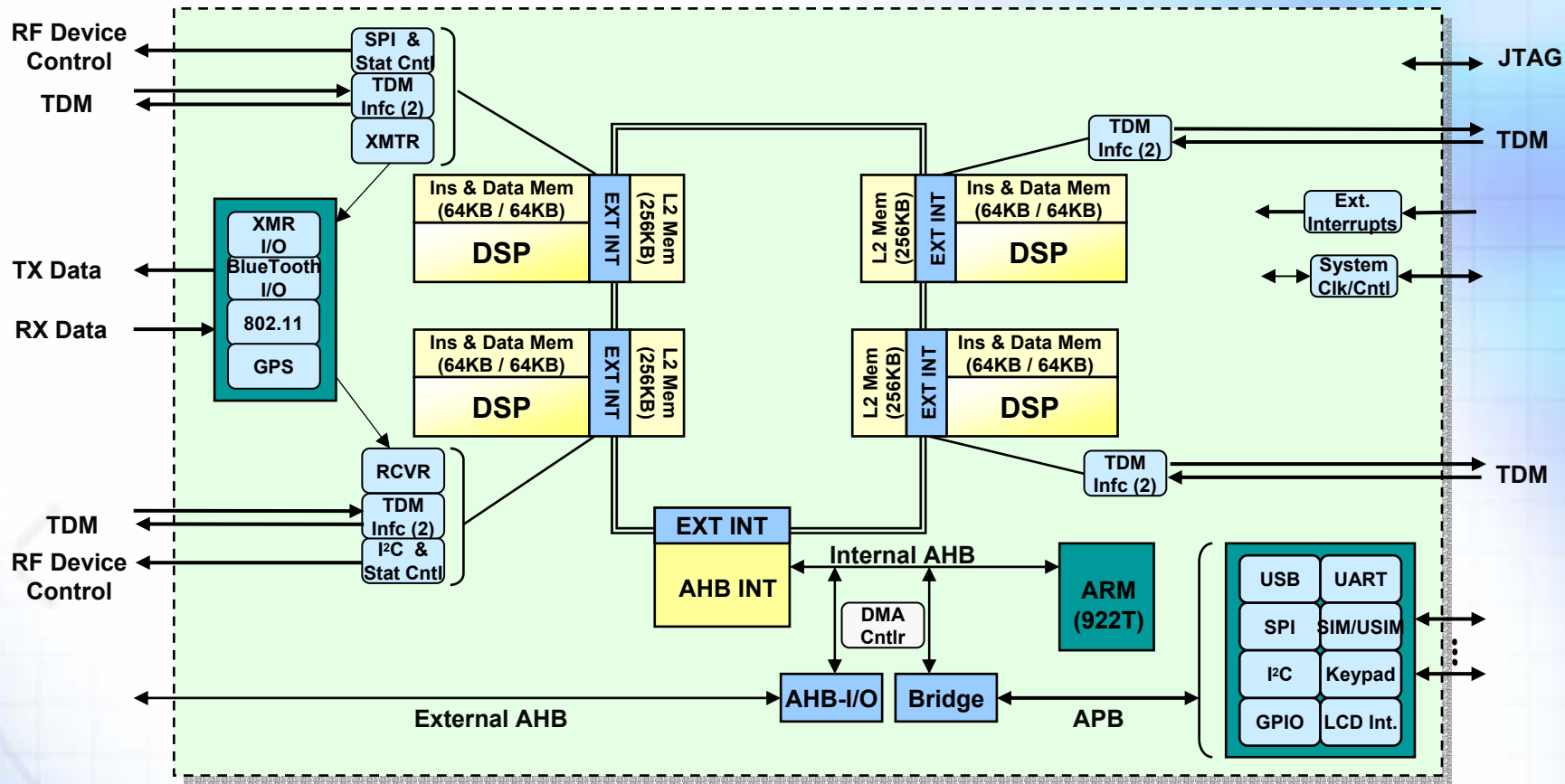
- ➔ MMS / SMS / iMode / WAP
- ➔ SIM / USIM
- ➔ SMIL / SyncML
- ➔ Java

## Reconfigurable on the Fly





# SB9600 2003 Handset Chip



- 0.13um CMOS, *custom*
- Replicated Sandblaster™ core
- Low Power design

# Summary

## Multithreaded baseband processor

- multi-threaded
- high-performance and low-power

## Sophisticated compiler technology

- automatically generates DSP operations
- near-assembly language performance

## Reconfigurable Communications Protocols

- WCDMA
- GSM, GPRS
- 802.11
- Bluetooth
- GPS



# Expanding the Dimensions of Wireless Multimedia Technology